Elektronische Bauelemente

SPT395N10V-C

395A, 100V, $R_{DS(ON)}$ 1.3mΩ
N-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

TOLL-8

FEATURES

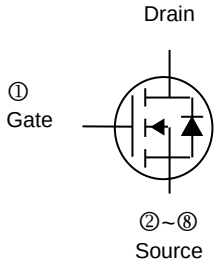
- Fast Switching
- Improved dv/dt Capability
- Green Device Available

APPLICATIONS

- Battery Management System
- Machine Tool
- High Power Inverter System

PACKAGE INFORMATION

Package	MPQ	Leader Size
TOLL-8	2K	13 inch



ORDER INFORMATION

Part Number	Type
SPT395N10V-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	395	A
Pulsed Drain Current [1]		I_{DM}	987	A
Power Dissipation	T_C=25℃	P_D	312.5	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient		$R_{\theta JA}$	40	℃/W
Thermal Resistance Junction-Case		$R_{\theta JC}$	0.4	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=80V, V_{GS}=0V
Static Drain-Source On-Resistance [3]	$R_{DS(ON)}$	-	-	1.3	mΩ	V_{GS}=10V, I_D=30A
Gate Resistance	R_g	-	1.7	-	Ω	V_{DS}=V_{GS}=0V, f=1MHz
Forward Transconductance	g_{fs}	-	108	-	S	V_{DS}=5V, I_D=50A
Total Gate Charge	Q_g	-	231	-	nC	V_{DD}=50V V_{GS}=10V I_D=100A
Gate-Source Charge	Q_{gs}	-	70.2	-		
Gate-Drain Change	Q_{gd}	-	65.7	-		
Turn-on Delay Time	$T_{d(on)}$	-	27.7	-	nS	V_{DD}=50V V_{GEN}=10V I_D=1A R_{GEN}=1Ω
Rise Time	T_r	-	21.5	-		
Turn-off Delay Time	$T_{d(off)}$	-	89.6	-		
Fall Time	T_f	-	96.8	-		
Input Capacitance	C_{iss}	-	13000	-	pF	V_{DS}=50V V_{GS}=0V f=1MHz
Output Capacitance	C_{oss}	-	2147	-		
Reverse Transfer Capacitance	C_{rss}	-	398	-		
Source-Drain Diode						
Continuous Source Current	I_S	-	-	85	A	V_D=V_G=0V, Force Current
Diode Forward Voltage	V_{SD}	-	-	1.1	V	I_S=30A, V_{GS}=0V
Reverse Recovery Time	t_{rr}	-	120	-	nS	I_{DS}=30A, V_{GS}=0V di/dt=100A/μs
Reverse Recovery Charge	Q_{rr}	-	400	-	nC	

Notes:

1. Repetitive Rating：Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed, pulse width≤300μs, duty cycle≤2%.
3. Guaranteed by design, not subject to production testing.

CHARACTERISTIC CURVES

FIG. 1-I_D vs T_C

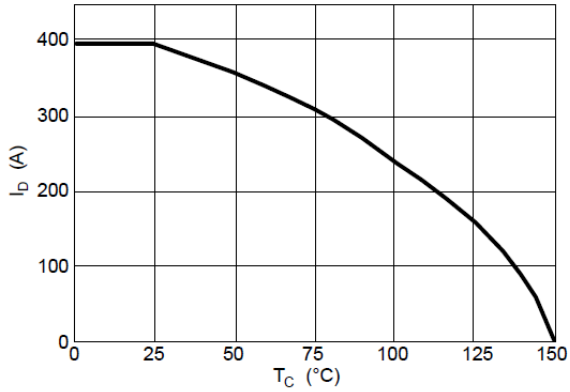


FIG. 2-Normalized $R_{DS(ON)}$ vs T_J

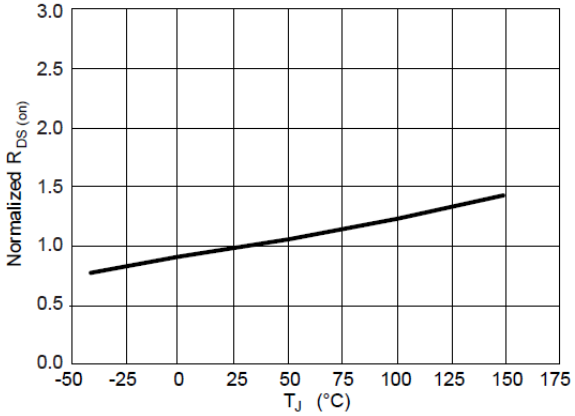


FIG. 3-Normalized $V_{GS(th)}$ vs T_J

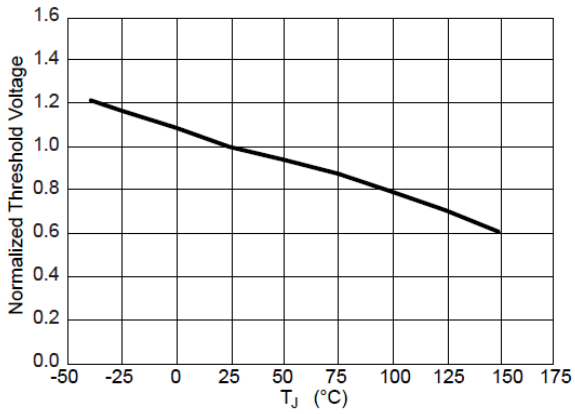


FIG. 4-Gate Charge Characteristics

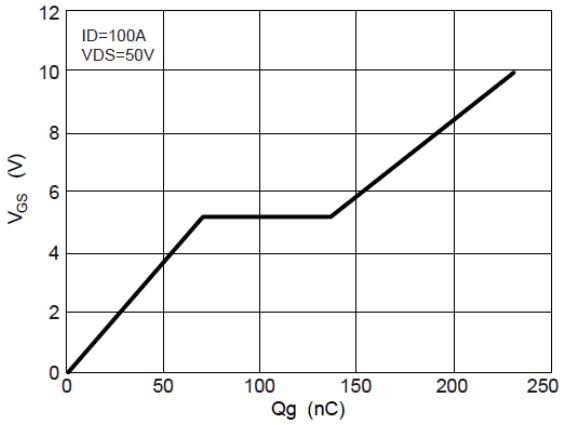


FIG. 5-$R_{DS(ON)}$ vs I_D

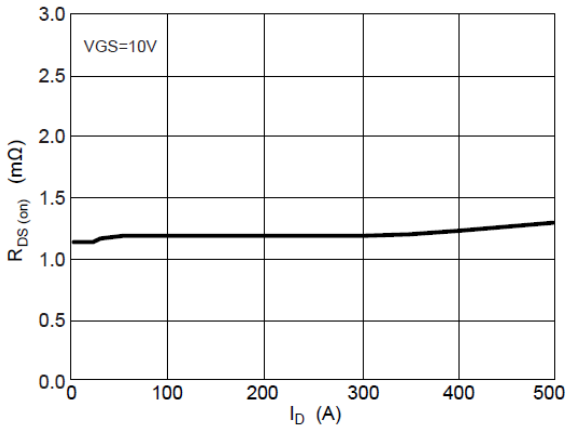
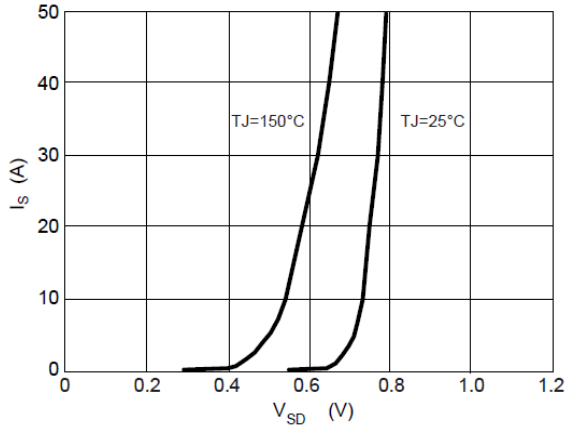


FIG. 6-I_S vs V_{SD}



CHARACTERISTIC CURVES

FIG. 7-Power Dissipation

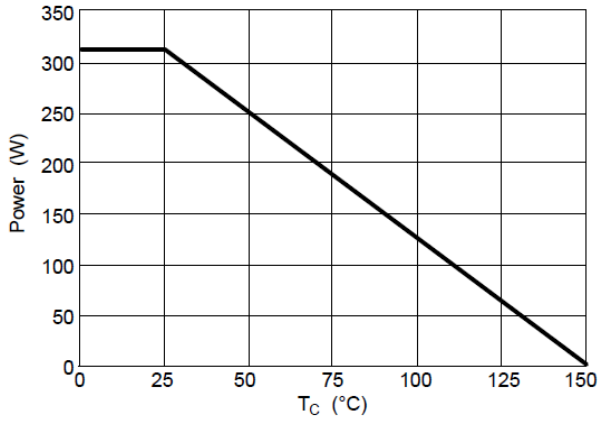


FIG. 8-Switching Time Waveform

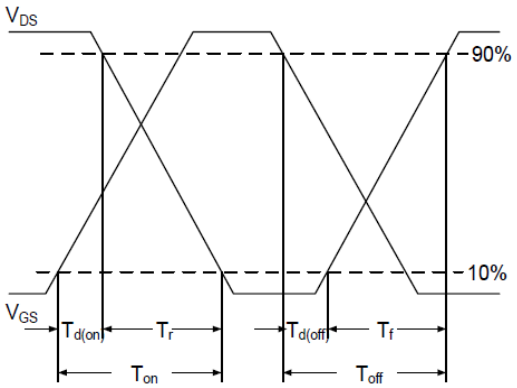
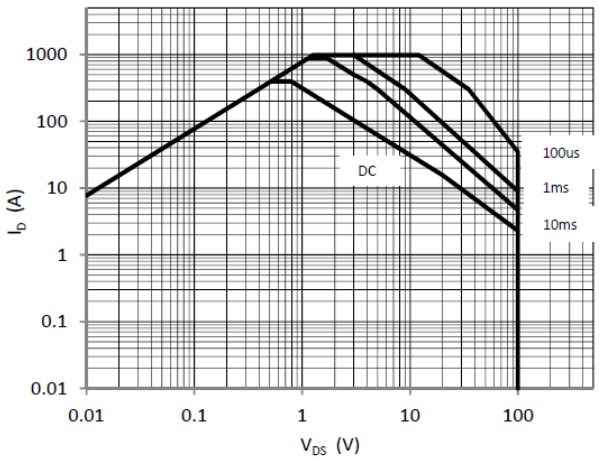
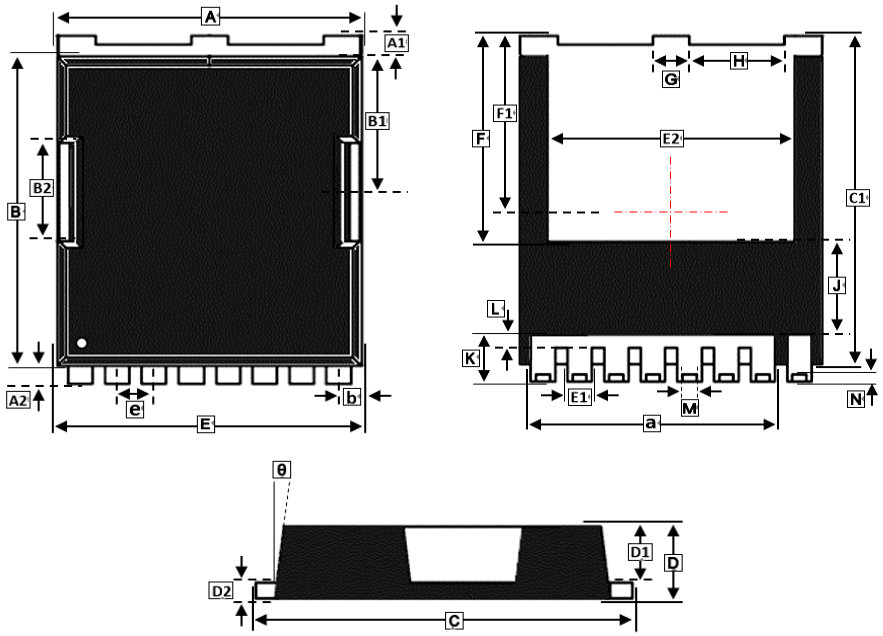


FIG. 9-Safe Operating Area



PACKAGE OUTLINE DIMENSIONS

TOLL-8



REF.	Millimeter	
	Min.	Max.
A	9.65	9.95
A1	0.50	0.90
A2	0.45	0.75
B	10.18	10.58
B1	4.45	4.65
B2	2.85	3.45
C	11.48	11.88
C1	10.98	11.18
D	2.15	2.45
D1	1.70	1.90
D2	0.40	0.60
E	9.70	10.10
E1	0.60	0.90
E2	7.95	9.25
F	6.95 BSC.	
F1	5.89 BSC.	
G	1.10	1.30
H	3.00	3.20
J	2.80 REF.	
K	1.40	2.10
L	0.30	0.80
M	0.46 REF.	
N	0.10 REF.	
θ	10° REF.	
a	8.00 REF.	
b	0.60	0.80
e	1.20 BSC.	

MOUNTING PAD LAYOUT

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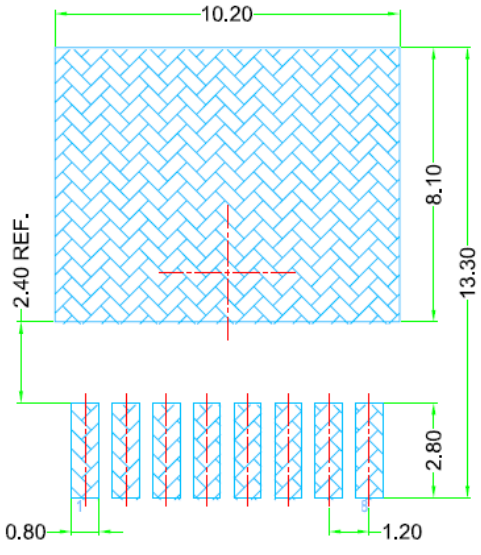

*Dimensions in millimeters