Elektronische Bauelemente

SPT367N10SV-C

367A, 100V, $R_{DS(ON)}$ 1.4mΩ

N-Channel Shielded Gate Trench Power MOSFET

RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using SGT MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

TOLL-8

FEATURES

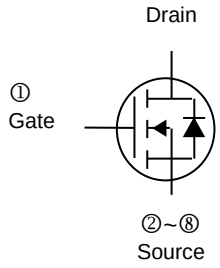
- 100% avalanche test
- Qualified According to JEDEC for Target Applications
- Green Device Available

APPLICATIONS

- Battery Protection
- Telecom and Server Power Supply
- Brushless DC Motor Control
- DC-DC Converters
- High Performance Synchronous Rectification
- Load Switch and eFuse

PACKAGE INFORMATION

Package	MPQ	Leader Size
TOLL-8	2K	13 inch



ORDER INFORMATION

Part Number	Type
SPT367N10SV-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @V_{GS}=10V [1]	T_C=25℃	I_D	367	A
	T_C=100℃		232	
Pulsed Drain Current [2]		I_{DM}	1471	A
Power Dissipation [4]	T_C=25℃	P_D	312	W
	T_A=25℃		3.12	
Single Pulsed Avalanche Energy [3]		E_{AS}	1440	mJ
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient [5]		$R_{\theta JA}$	40	℃/W
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	0.4	

ELECTRICAL CHARACTERISTICS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
Drain-Source Leakage Current	T_C=25℃	I_{DSS}	-	-	1	uA	V_{DS}=100V, V_{GS}=0V
	T_C=55℃		-	-	10		
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	1.1	1.4	mΩ	V_{GS}=10V, I_D=150A
			-	1.6	2		V_{GS}=6V, I_D=75A
Gate Resistance		R_g	-	0.6	-	Ω	
Forward Transconductance		g_{fs}	-	312	-	S	V_{DS}=1V, I_D=150A
Total Gate Charge		Q_g	-	141	-	nC	V_{DD}=50V V_{GS}=10V I_D=100A
Gate-Source Charge		Q_{gs}	-	45	-		
Gate-Drain Change		Q_{gd}	-	33	-		
Turn-on Delay Time		$T_{d(on)}$	-	39	-	nS	V_{DD}=50V V_{GS}=10V I_D=100A R_G=1Ω
Rise Time		T_r	-	37	-		
Turn-off Delay Time		$T_{d(off)}$	-	45	-		
Fall Time		T_f	-	13	-		
Input Capacitance		C_{iss}	-	10043	-	pF	V_{DS}=50V V_{GS}=0V f=1MHz
Output Capacitance		C_{oss}	-	4487	-		
Reverse Transfer Capacitance		C_{rss}	-	70	-		
Source-Drain Diode							
Continuous Source Current [1 6]		I_S	-	-	260	A	V_D=V_G=0V, Force Current
Pulsed Source Current [2 6]		I_{SM}	-	-	1471		
Diode Forward Voltage [2]		V_{SD}	-	0.84	-	V	I_S=100A, V_{GS}=0V T_J=25℃
Reverse Recovery Time		t_{rr}	-	65	-	nS	I_S=100A, di/dt=400A/μs T_J=25℃
Reverse Recovery Charge		Q_{rr}	-	480	-	nC	

Notes:

1. The data tested by surface mounted on one inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width≤300μs, duty cycle≤2%.
3. The E_{AS} data shows Max. rating. The test condition is L=0.5mH, I_{AS}=75.8A.
4. The power dissipation is limited by 150℃ juncti on temperature.
5. Mounted on 1 inch square PCB
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

TYPICAL CHARACTERISTICS

Fig 1. Output Characteristics, T_J=25℃

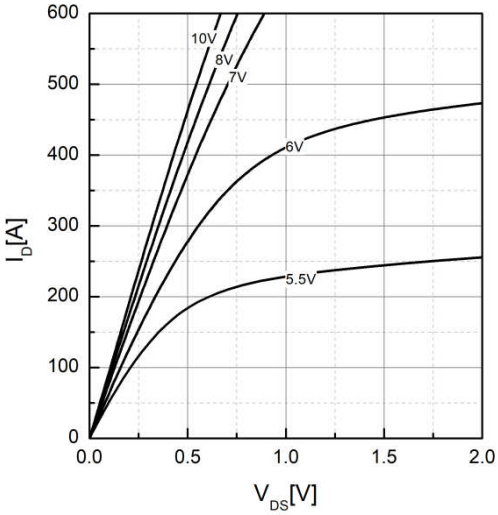


Fig 2. Drain-source on resistance, T_J=25℃

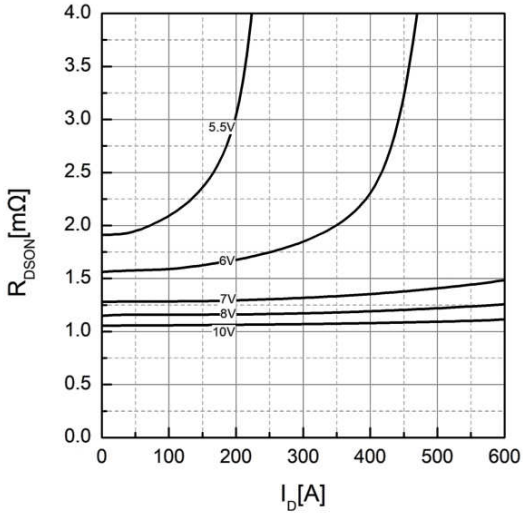


Fig 3. Forward characteristics of body diode

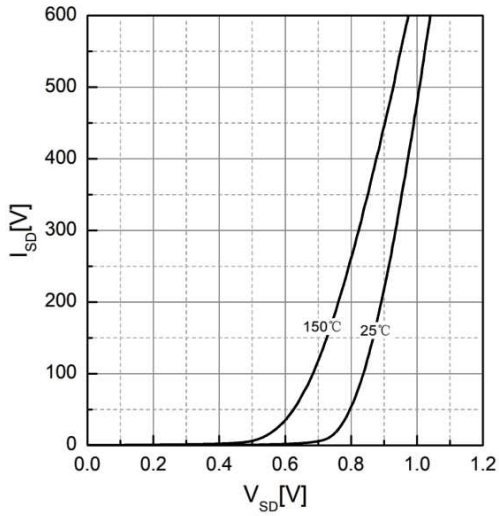


Fig 4. Gate Charge Characteristics

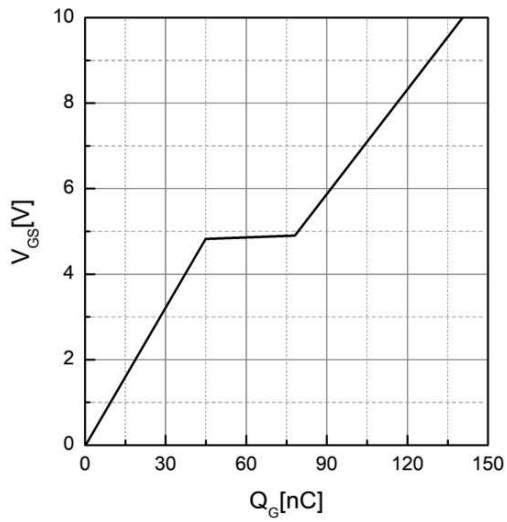


Fig 5. Capacitance Characteristics

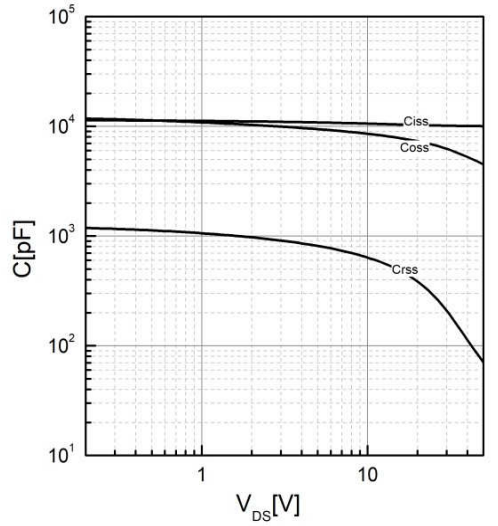
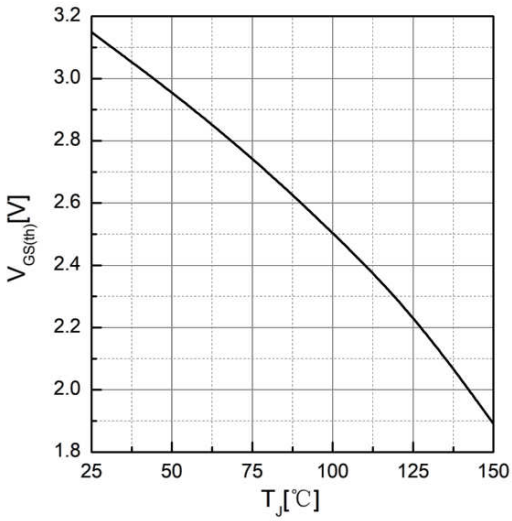


Fig 6. Threshold Voltage Vs. Temperature



TYPICAL CHARACTERISTICS

Fig 7. Drain-source on-state resistance

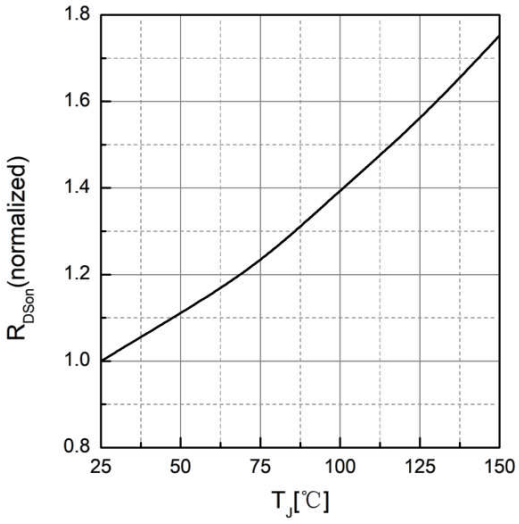


Fig 8. Maximum Safe Operating Area

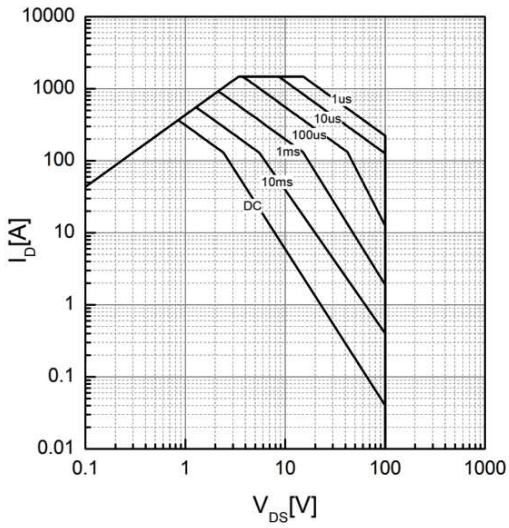


Fig 9. Avalanche characteristics

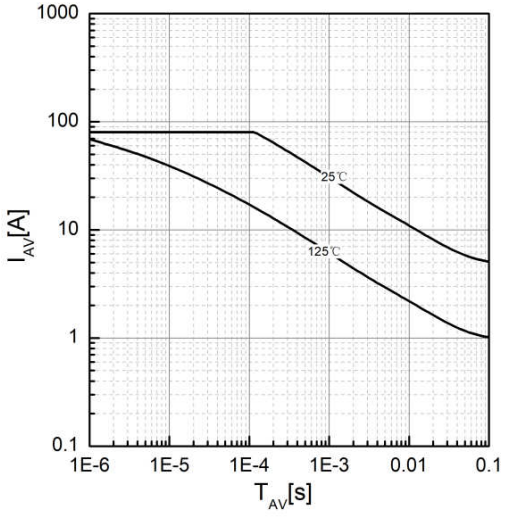


Fig 10. Drain-source breakdown voltage

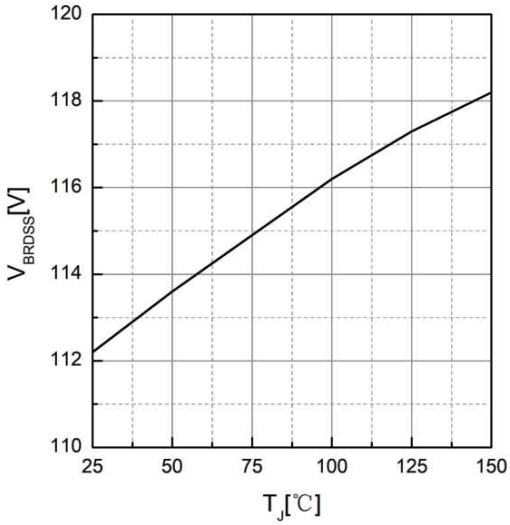


Fig 11. Transfer characteristics

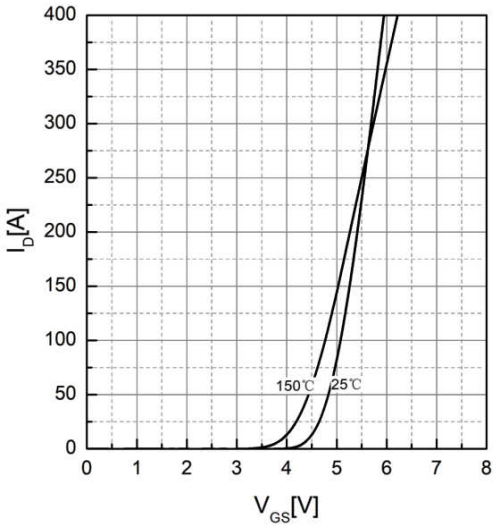
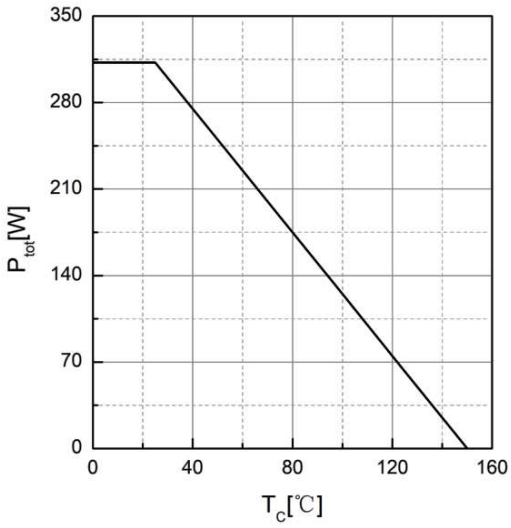


Fig 12. Power dissipation



TYPICAL CHARACTERISTICS

Fig 13. Drain current

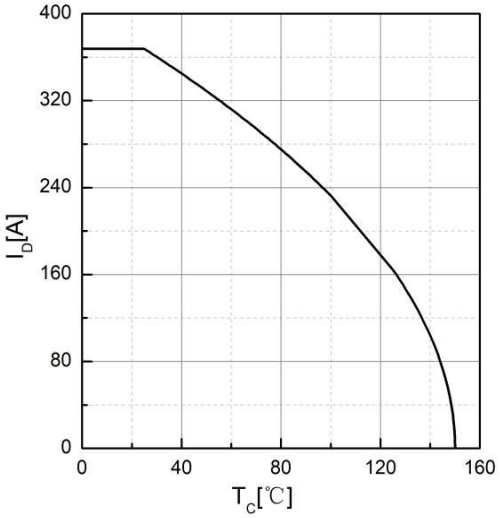


Fig 14. Effective Transient Thermal Impedance

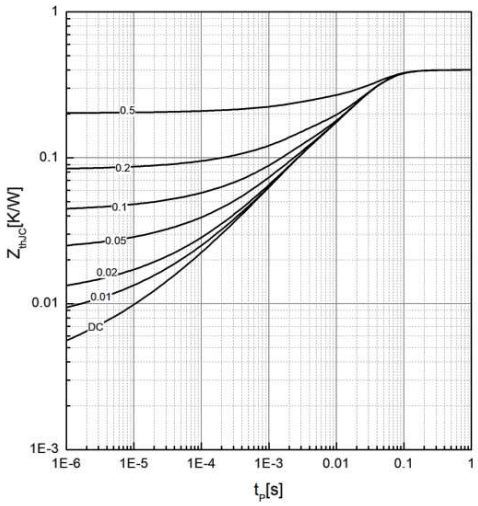


Fig 15. Gate Charge Test Circuit & Waveform

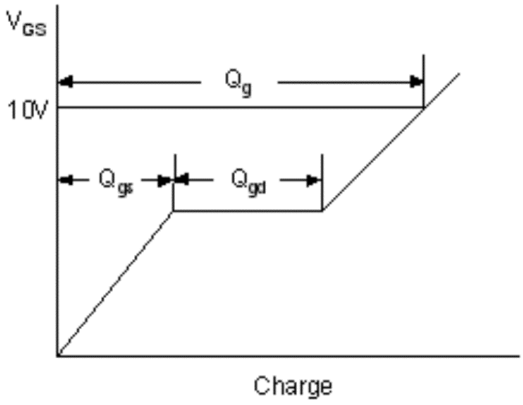


Fig 16. Resistive Switching Test Circuit & Waveforms

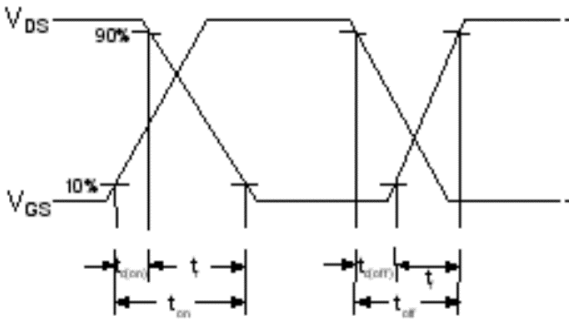
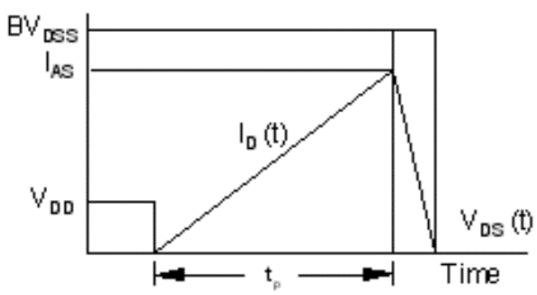


Fig 17. Unclamped Inductive Switching
Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$



PACKAGE OUTLINE DIMENSIONS

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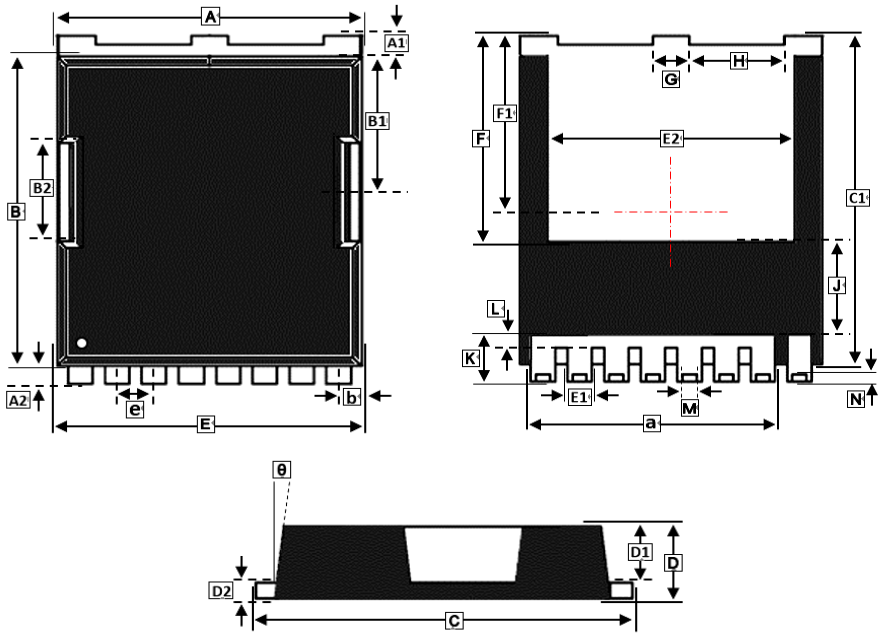

REF.	Millimeter	
	Min.	Max.
A	9.65	9.95
A1	0.50	0.90
A2	0.45	0.75
B	10.18	10.58
B1	4.45	4.65
B2	2.85	3.45
C	11.48	11.88
C1	10.98	11.18
D	2.15	2.45
D1	1.70	1.90
D2	0.40	0.60
E	9.70	10.10
E1	0.60	0.90
E2	7.95	9.25
F	6.95 BSC.	
F1	5.89 BSC.	
G	1.10	1.30
H	3.00	3.20
J	2.80 REF.	
K	1.40	2.10
L	0.30	0.80
M	0.46 REF.	
N	0.10 REF.	
θ	10° REF.	
a	8.00 REF.	
b	0.60	0.80
e	1.20 BSC.	

MOUNTING PAD LAYOUT

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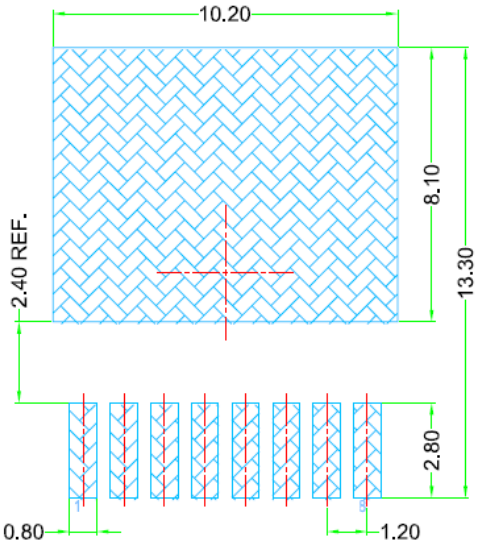

*Dimensions in millimeters