

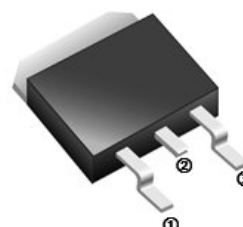
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSU206N15SV-C is the Shielded Gate Technology N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSU206N15SV-C meet the RoHS and Green Product requirement with full function reliability approved.

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FEATURES

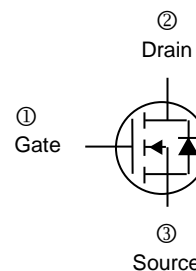
- Shielded Gate Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING



PACKAGE INFORMATION

| Package | MPQ | Leader Size |
|---------|------|-------------|
| TO-263 | 0.8K | 13 inch |



ORDER INFORMATION

| Part Number | Type |
|---------------|---------------------------------|
| SSU206N15SV-C | Lead (Pb)-free and Halogen-free |

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Rating | Unit |
|---|------------------------|-------------------------|--------------------|
| Drain-Source Voltage | V_{DS} | 150 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current ¹ (Silicon Limited) | I_D | $T_C=25^\circ\text{C}$ | 206 |
| | | $T_C=100^\circ\text{C}$ | 146 |
| Continuous Drain Current ¹ (Package Limited) | $T_C=25^\circ\text{C}$ | 180 | A |
| Pulsed Drain Current ² | I_{DM} | 650 | A |
| Power Dissipation | $T_C=25^\circ\text{C}$ | P_D | 429 |
| Operating Junction & Storage Temperature Range | T_J, T_{STG} | -55~175 | $^\circ\text{C}$ |
| Thermal Resistance Rating | | | |
| Thermal Resistance Junction-Ambient ¹ | $R_{\theta JA}$ | 60 | $^\circ\text{C/W}$ |
| Thermal Resistance Junction-Case ¹ | $R_{\theta JC}$ | 0.35 | |

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|--|---------------|-------------------------|------|-----------|------------|---|--------------------------|
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | 150 | - | - | V | $V_{GS}=0V, I_D=250\mu A$ | |
| Gate-Threshold Voltage | $V_{GS(th)}$ | 2 | - | 4 | V | $V_{DS}=V_{GS}, I_D=250\mu A$ | |
| Forward Transfer Conductance | g_{fs} | - | 70 | - | S | $V_{DS}=5V, I_D=20A$ | |
| Gate-Source Leakage Current | I_{GSS} | - | - | ± 100 | nA | $V_{GS}=\pm 20V$ | |
| Drain-Source Leakage Current | I_{DSS} | $T_J=25^\circ\text{C}$ | - | - | 1 | μA | $V_{DS}=150V, V_{GS}=0V$ |
| | | $T_J=100^\circ\text{C}$ | - | - | 100 | | |
| Static Drain-Source On-Resistance ³ | $R_{DS(ON)}$ | - | 3.9 | 4.3 | m Ω | $V_{GS}=10V, I_D=20A$ | |
| Gate Resistance | R_g | - | 4 | - | Ω | $f=1\text{MHz}$ | |
| Total Gate Charge | Q_g | - | 70 | - | nC | $I_D=20A$ $V_{DD}=75V$ $V_{GS}=10V$ | |
| Gate-Source Charge | Q_{gs} | - | 20 | - | | | |
| Gate-Drain Change | Q_{gd} | - | 10 | - | | | |
| Turn-on Delay Time | $T_{d(on)}$ | - | 19 | - | nS | $V_{DD}=75V$ $I_D=20A$ $V_{GS}=10V$ $R_G=10\Omega$ | |
| Rise Time | T_r | - | 24 | - | | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 35 | - | | | |
| Fall Time | T_f | - | 11 | - | | | |
| Input Capacitance | C_{iss} | - | 5230 | - | pF | $V_{GS}=0V$ $V_{DS}=75V$ $f=1\text{MHz}$ | |
| Output Capacitance | C_{oss} | - | 745 | - | | | |
| Reverse Transfer Capacitance | C_{rss} | - | 11.5 | - | | | |
| Source-Drain Diode | | | | | | | |
| Diode Forward Voltage ³ | V_{SD} | - | 0.9 | - | V | $I_F=20A, V_{GS}=0V$ | |
| Reverse Recovery Time | T_{rr} | - | 120 | - | nS | $I_F=20A, V_R=75V$ $di_F/dt=100A/\mu s$ | |
| Reverse Recovery Charge | Q_{rr} | - | 270 | - | nC | | |

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
3. The Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

CHARACTERISTIC CURVES

Fig 1. Typical Output Characteristics

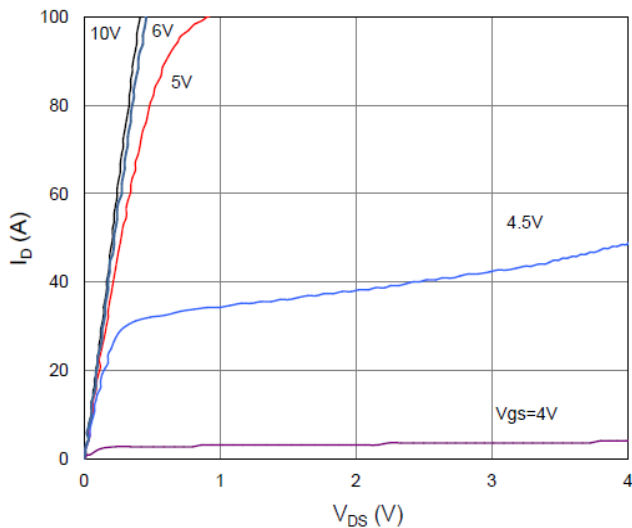


Figure 2. On-Resistance vs. Gate-Source Voltage

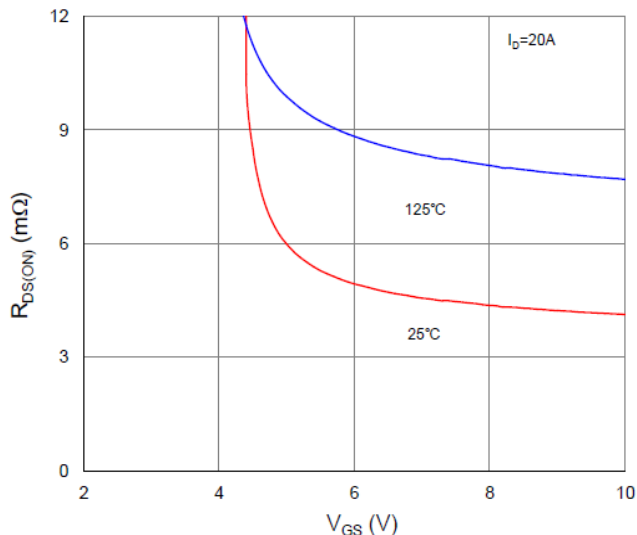


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

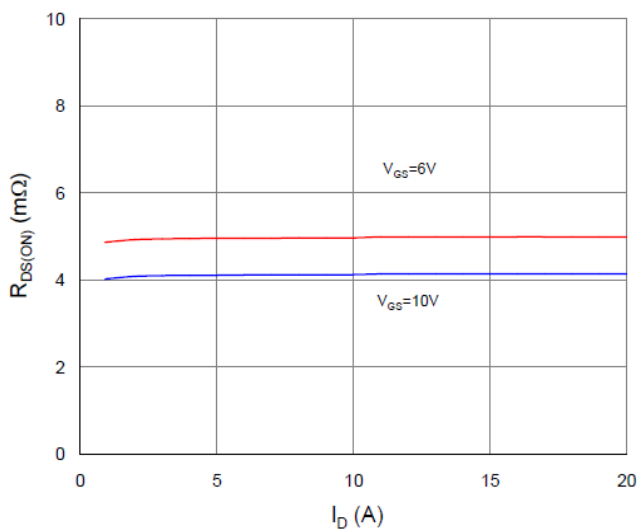


Figure 4. Normalized On-Resistance vs. Junction Temperature

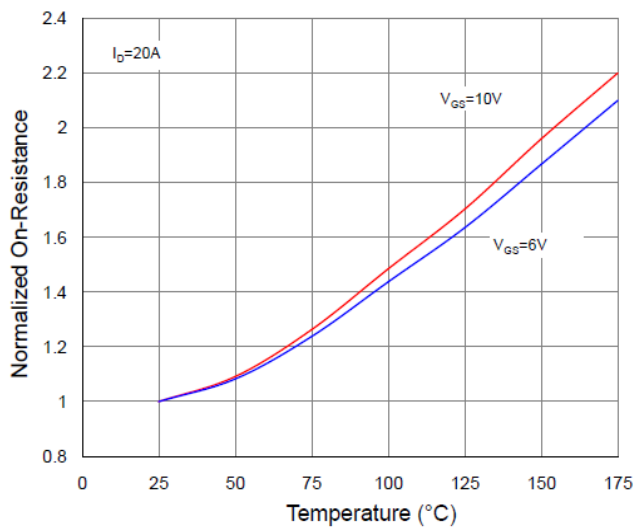


Figure 5. Typical Transfer Characteristics

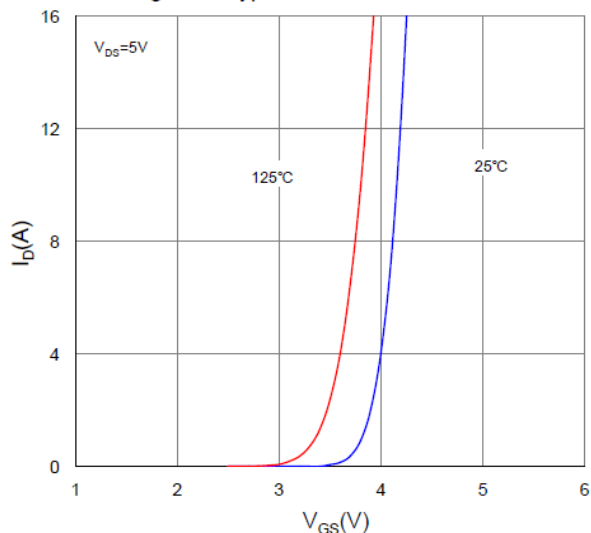
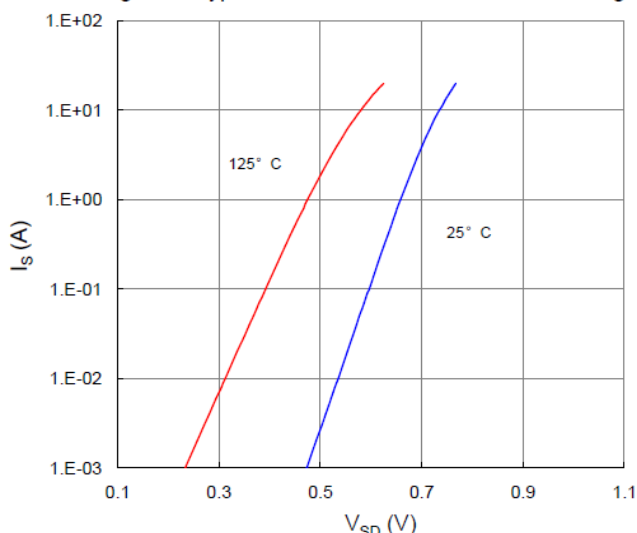


Figure 6. Typical Source-Drain Diode Forward Voltage



CHARACTERISTIC CURVES

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

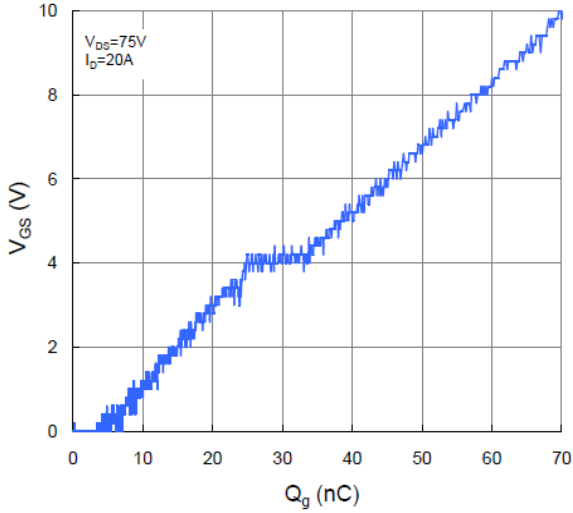


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

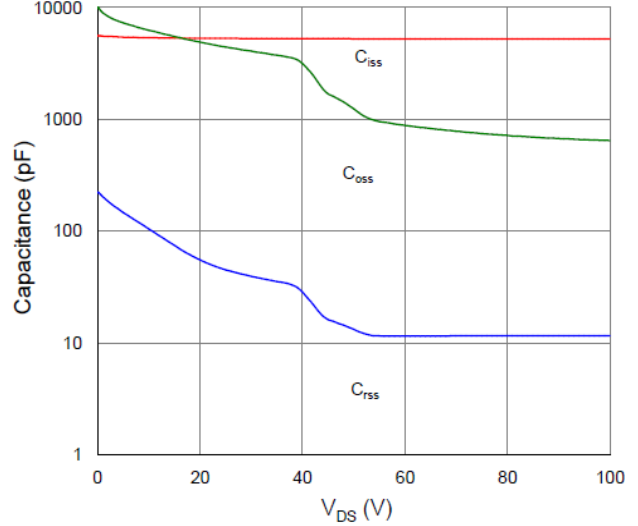


Figure 9. Maximum Safe Operating Area

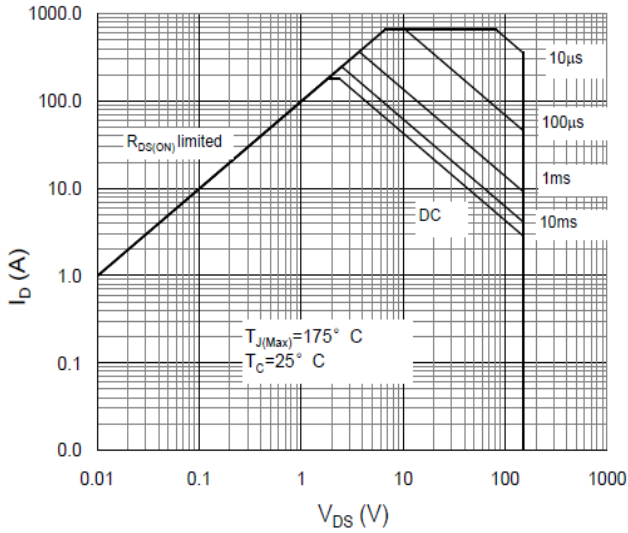


Figure 10. Maximum Drain Current vs. Case Temperature

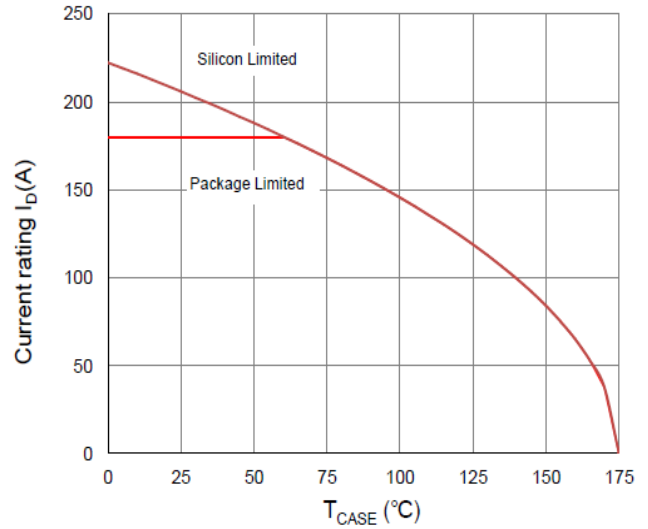
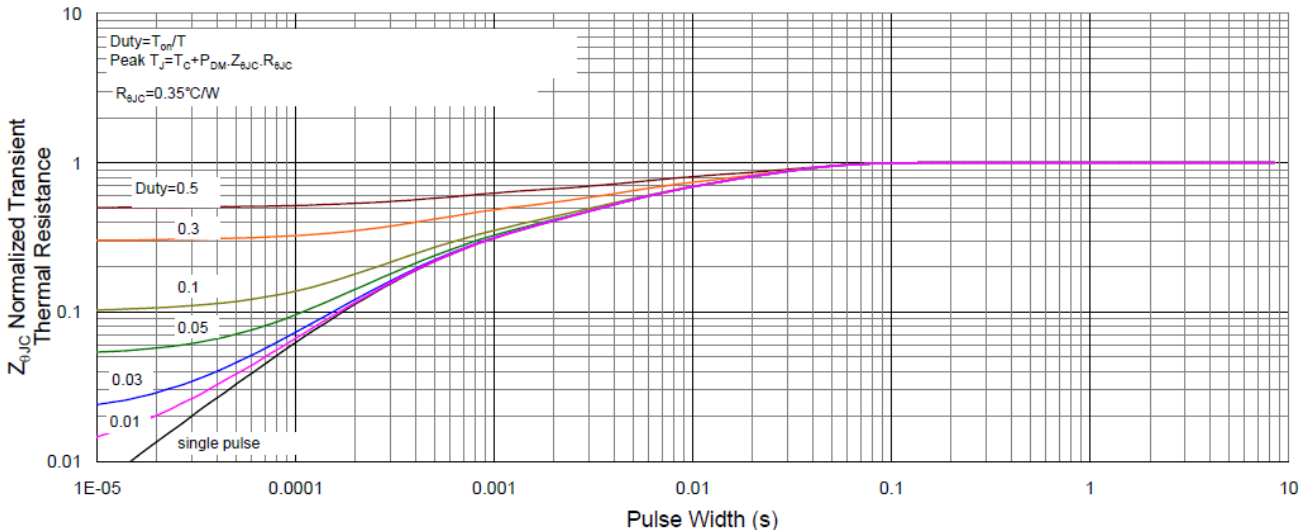
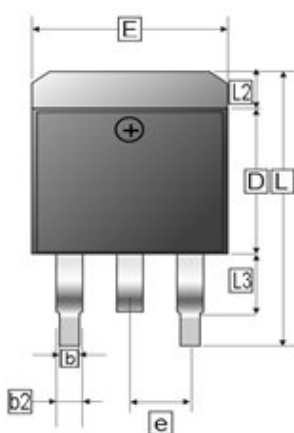


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



PACKAGE OUTLINE DIMENSIONS

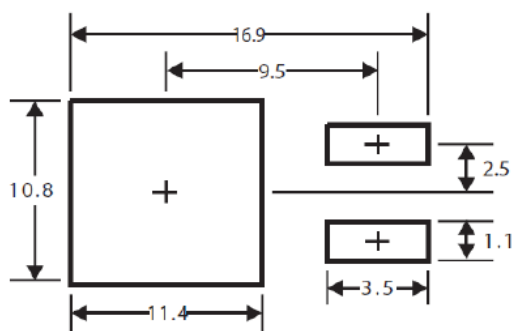
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| REF. | Millimeter | |
|------|------------|-------|
| | Min. | Max. |
| A | 4.00 | 4.87 |
| b | 0.508 | 1.01 |
| L4 | 0 | 0.30 |
| C | 0.30 | 0.74 |
| L3 | 1.50 REF. | |
| L1 | 2.50 REF. | |
| E | 9.60 | 10.67 |
| c2 | 1.07 | 1.65 |
| b2 | 1.34 REF. | |
| D | 8.00 | 9.652 |
| e | 2.54 REF. | |
| L | 14.6 | 16.1 |
| L2 | 1.27 REF. | |

MOUNTING PAD LAYOUT

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*Dimensions in millimeters