Elektronische Bauelemente

SSD90N12S-C

90A, 120V, $R_{DS(ON)}$ 9mΩ

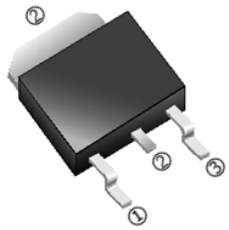
N-Channel Shielded Gate Trench Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD90N12S-C uses advanced SGT II technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 7.5V. This device is suitable for use as a Battery protection or in other Switching application.

TO-252(D-Pack)

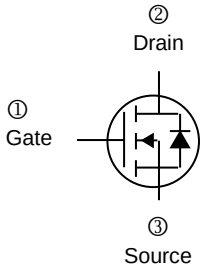


APPLICATION

- Mobile phone fast charging
- Brushless motor
- Home appliance control board

PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch



ORDER INFORMATION

Part Number	Type
SSD90N12S-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	120	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_C=25℃	I_D	90	A
	T_C=75℃		35	
Pulsed Drain Current [2]	T_C=25℃	I_{DM}	270	A
Power Dissipation [3]	T_C=25℃	P_D	140	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Thermal Resistance Junction-Ambient [4]		$R_{\theta JA}$	62.5	℃/W
Thermal Resistance Junction-Case		$R_{\theta JC}$	0.89	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	120	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	1.5	2.0	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V, V_{DS}=0V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=120V, V_{GS}=0
	T_J=100℃		-	-	100		
Static Drain-Source On-Resistance		$R_{DS(ON)}$	-	7.5	9	mΩ	V_{GS}=10V, I_D=20A
			-	9	12		V_{GS}=4.5V, I_D=10A
Gate Resistance		R_g	-	2.3	-	Ω	f=1MHz
Forward Transconductance		gfs	-	75	-	S	V_{DS}= 10V, I_D=20A
Total Gate Charge		Q_g	-	30	-	nC	V_{DS}=60V V_{GS}=10V I_D=20A
Gate-Source Charge		Q_{gs}	-	5.8	-		
Gate-Drain Change		Q_{gd}	-	6	-		
Turn-on Delay Time		$T_{d(on)}$	-	9.5	-	nS	V_{DD}=60V V_{GS}=10V I_D=20A R_G=3Ω
Rise Time		T_r	-	4.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	27.2	-		
Fall Time		T_f	-	6.6	-		
Input Capacitance		C_{iss}	-	1854	-	pF	V_{DS}=60V V_{GS}=0 f=1MHz
Output Capacitance		C_{oss}	-	270	-		
Reverse Transfer Capacitance		C_{rss}	-	10	-		
Source-Drain Diode							
Continuous Source Current		I_S	-	-	90	A	T_C=25℃
Diode Forward Voltage		V_{SD}	-	-	1.2	V	I_S=20A, V_{GS}=0
Reverse Recovery Time		T_{rr}	-	52	-	nS	I_F=20A, di/dt=100A/μs
Reverse Recovery Charge		Q_{rr}	-	83.5	-	nC	

Notes:
1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width.
3. The power dissipation is limited by 175℃ juncti on temperature.
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

Fig 1. Output Characteristics

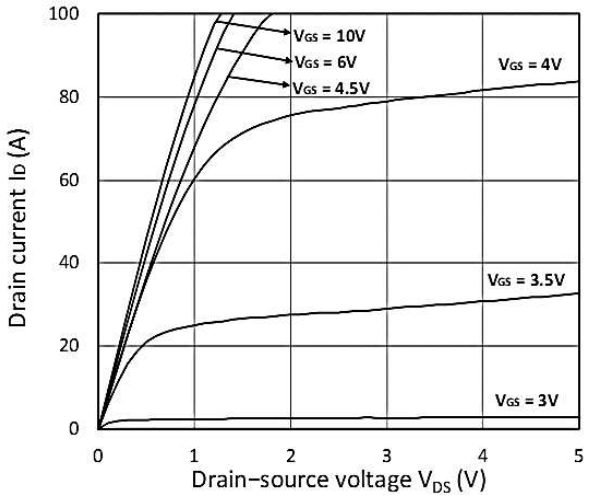


Fig 2. Transfer Characteristics

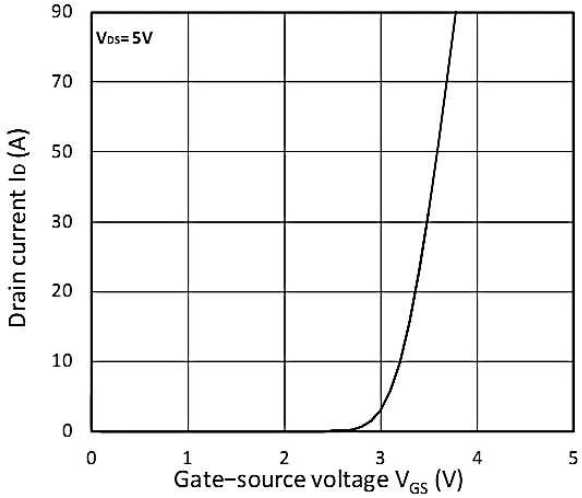


Fig 3. Forward Characteristics of Reverse

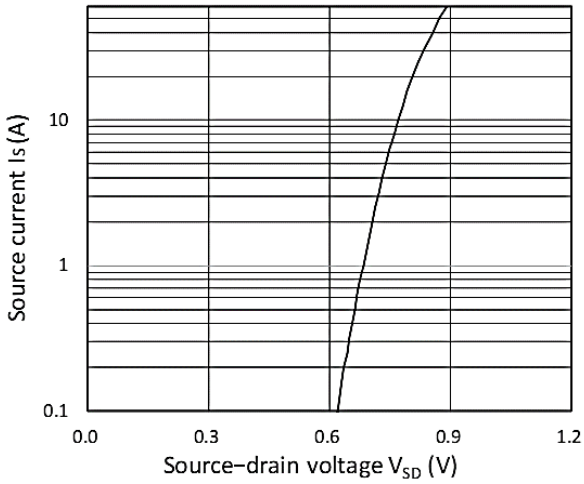


Fig 4. $R_{DS(ON)}$ vs. V_{GS}

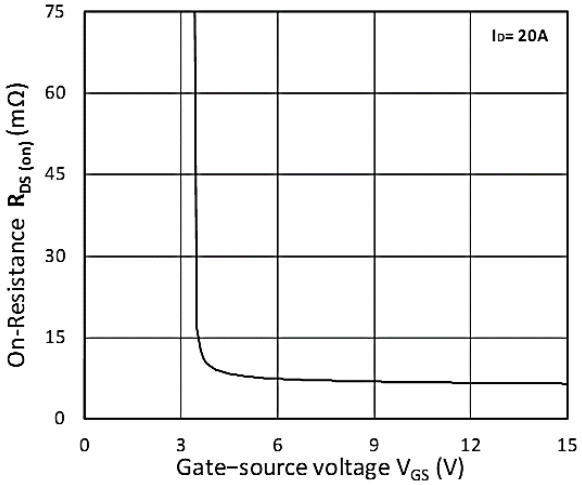


Fig 5. $R_{DS(ON)}$ vs. I_D

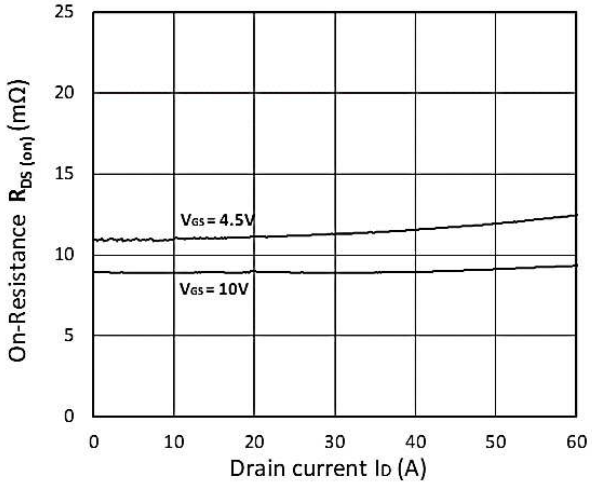
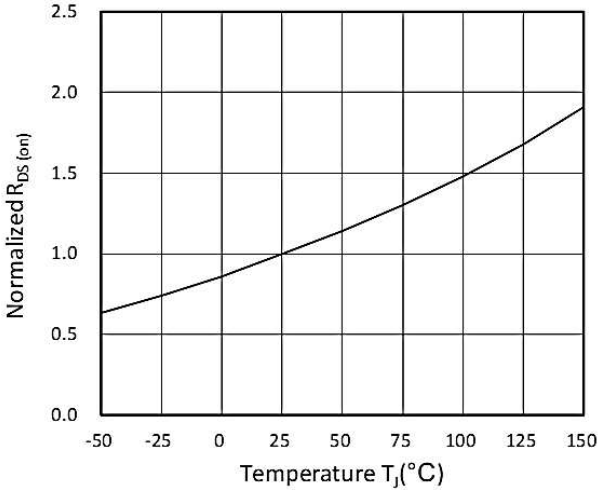


Fig 6. Normalized $R_{DS(ON)}$ vs. Temperature



CHARACTERISTIC CURVES

Fig 7. Capacitance Characteristics

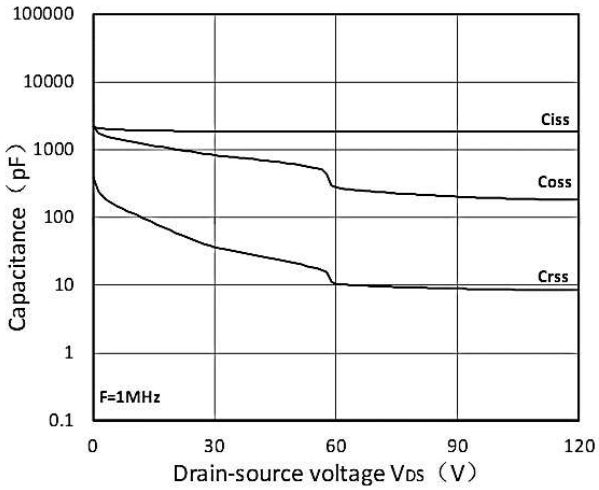


Fig 8. Gate Charge Characteristics

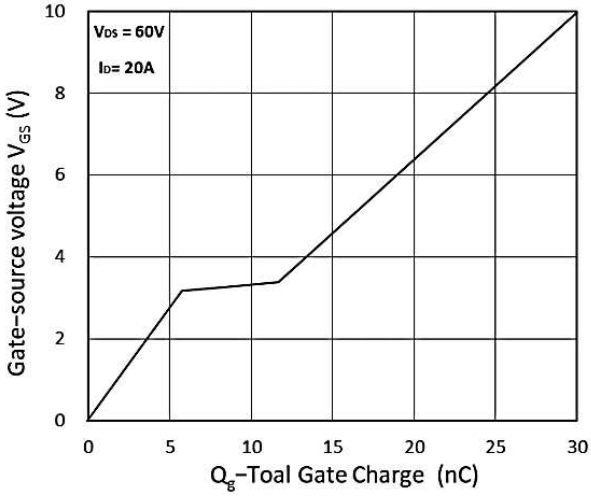


Fig 9. Power Dissipation

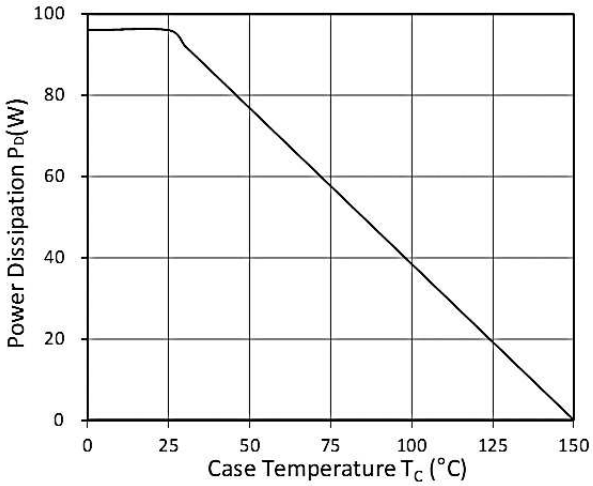


Fig 10. Safe Operating Area

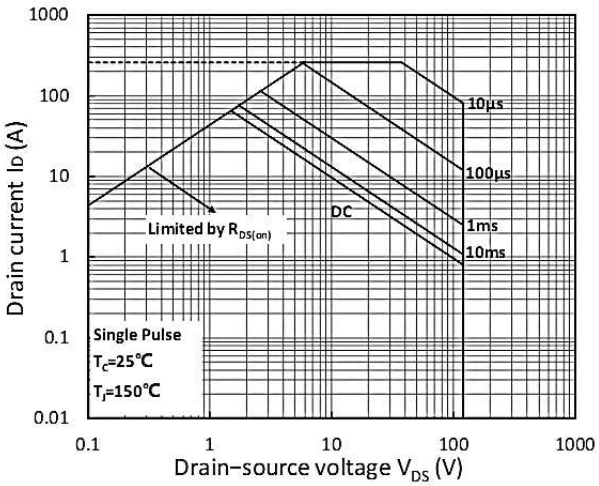
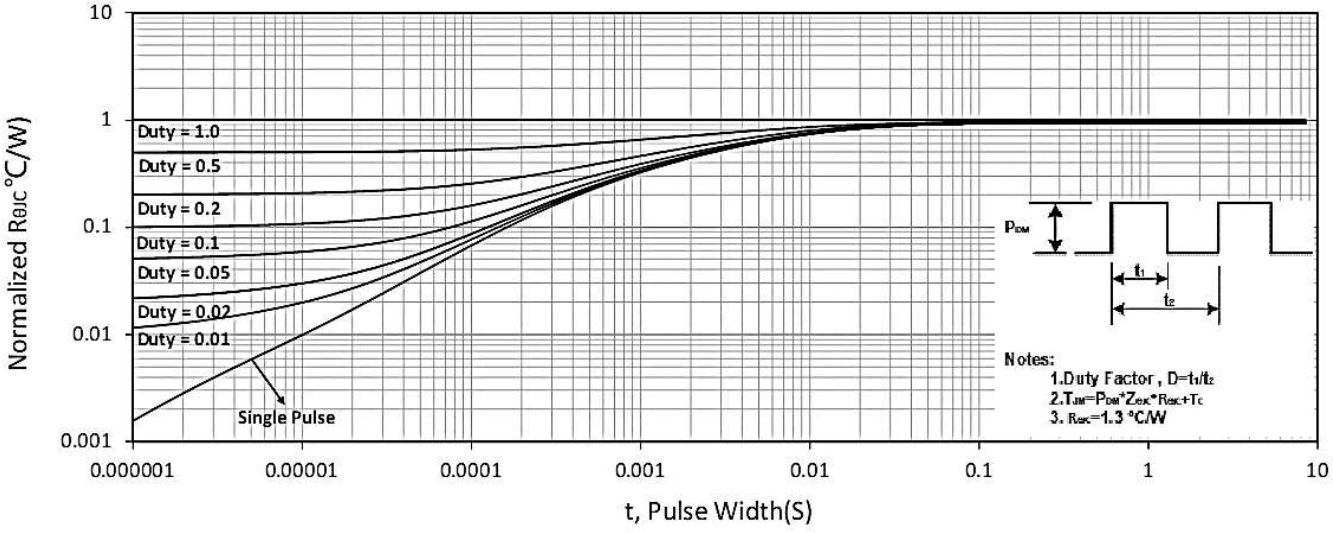
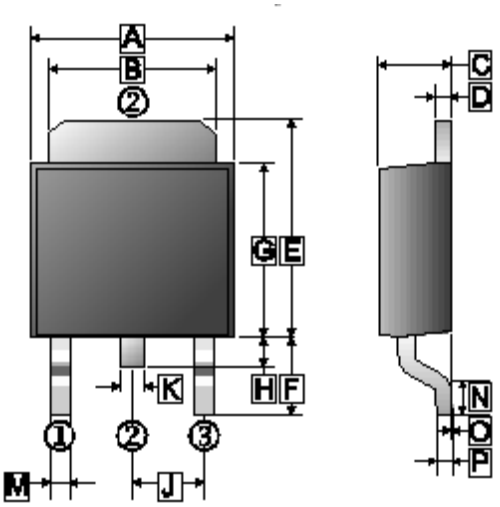


Fig 11. Normalized Maximum Transient Thermal Impedance



PACKAGE OUTLINE DIMENSIONS

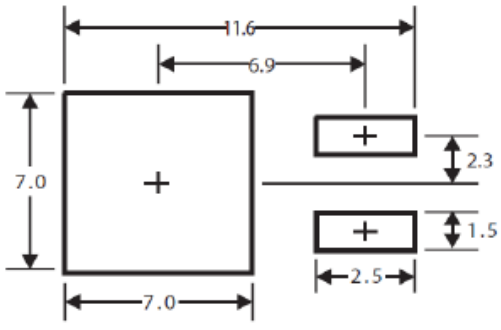
TO-252



REF.	Millimeter	
	Min.	Max.
A	6.30	6.90
B	4.95	5.53
C	2.10	2.50
D	0.35	0.90
E	6.00	7.70
F	2.90 REF.	
G	5.30	6.40
H	0.60	1.20
J	2.30 REF.	
K	0.89 REF.	
M	0.45	1.14
N	1.55 TYP.	
O	0	0.15
P	0.58 REF.	

MOUNTING PAD LAYOUT

TO-252



*Dimensions in millimeters