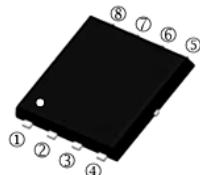


RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching application.

SPR-8PP



FEATURES

- Improved dv/dt capability
- Fast switching
- Green Device Available

APPLICATION

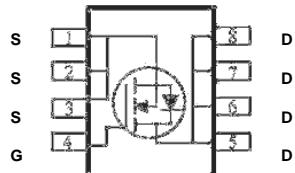
- Networking
- Load Switch
- LED applications

MARKING

NC2P6

PACKAGE INFORMATION

Package	MPQ	Leader Size
SPR-8PP	3K	13 inch



ORDER INFORMATION

Part Number	Type
SSPR90N03-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_c=25^\circ\text{C}$	I_D	90	A
Pulsed Drain Current ¹	I_{DM}	360	A
Power Dissipation $T_c=25^\circ\text{C}$	P_D	51	W
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55~150	°C
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62	°C/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	2.43	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(\text{th})}$	1.2	-	2.5	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$
Drain-Source Leakage Current	$I_{DS(on)}$	-	-	1	μA	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	-	-	2.6	m Ω	$V_{GS}=10\text{V}$, $I_D=20\text{A}$
		-	-	5		$V_{GS}=4.5\text{V}$, $I_D=15\text{A}$
Gate Resistance	R_g	-	1	-	Ω	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$
Forward Transconductance	g_{fs}	-	7	-	S	$V_{DS}=10\text{V}$, $I_D=3\text{A}$
Total Gate Charge	Q_g	-	24	-	nC	$V_{DS}=15\text{V}$
Gate-Source Charge	Q_{gs}	-	5.8	-		$V_{GS}=10\text{V}$
Gate-Drain Change	Q_{gd}	-	4.5	-		$I_D=45\text{A}$
Turn-on Delay Time	$T_{d(on)}$	-	4	-	nS	$V_{DD}=15\text{V}$
Rise Time	T_r	-	6	-		$V_{GS}=10\text{V}$
Turn-off Delay Time	$T_{d(off)}$	-	12	-		$I_D=45\text{A}$
Fall Time	T_f	-	8	-		$R_G=6\Omega$
Input Capacitance	C_{iss}	-	1870	-	pF	$V_{DS}=15\text{V}$
Output Capacitance	C_{oss}	-	1380	-		$V_{GS}=0\text{V}$
Reverse Transfer Capacitance	C_{rss}	-	18	-		$f=1\text{MHz}$
Source-Drain Diode						
Continuous Source Current	I_s	-	-	90	A	$V_G=V_D=0\text{V}$, Force Current
Diode Forward Voltage	V_{SD}	-	-	1	V	$I_s=1\text{A}$, $V_{GS}=0\text{V}$

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

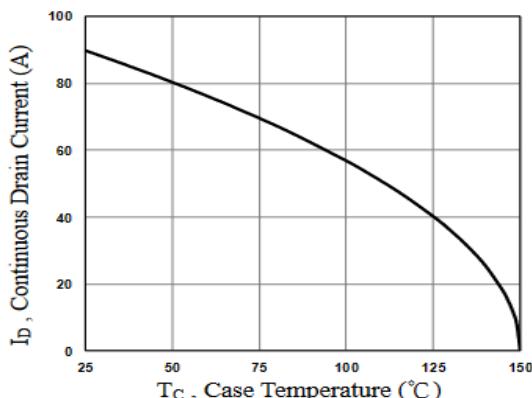


Fig.1 Continuous Drain Current vs. T_c

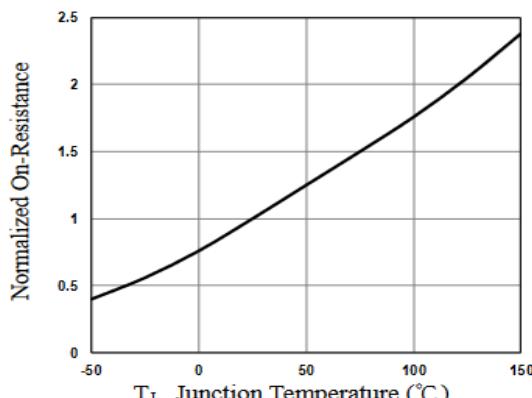


Fig.2 Normalized $R_{DS(ON)}$ vs. T_j

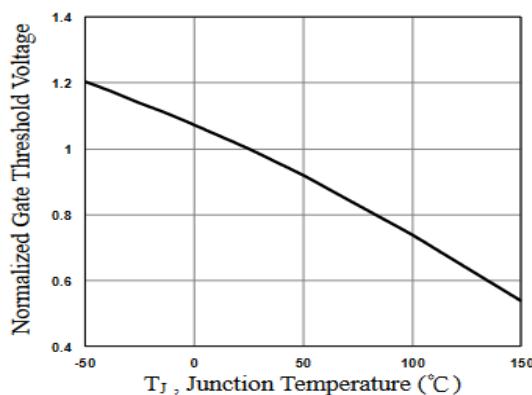


Fig.3 Normalized V_{th} vs. T_j

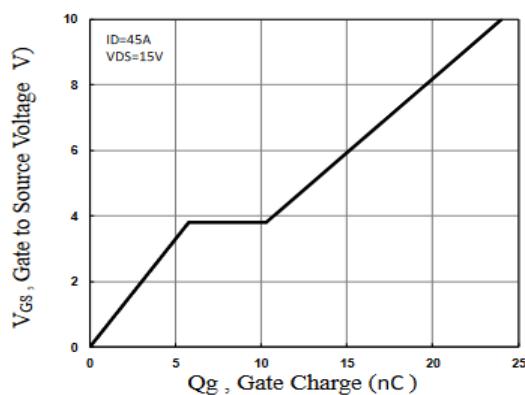


Fig.4 Gate Charge Characteristics

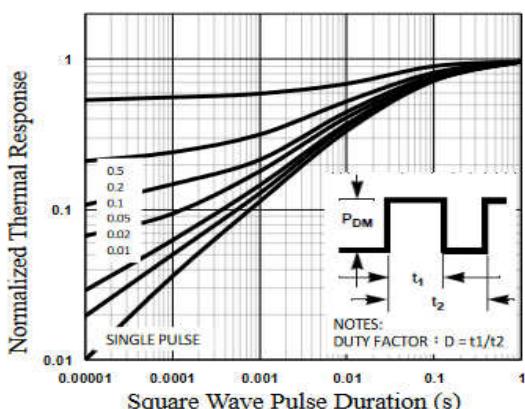


Fig.5 Normalized Transient Impedance

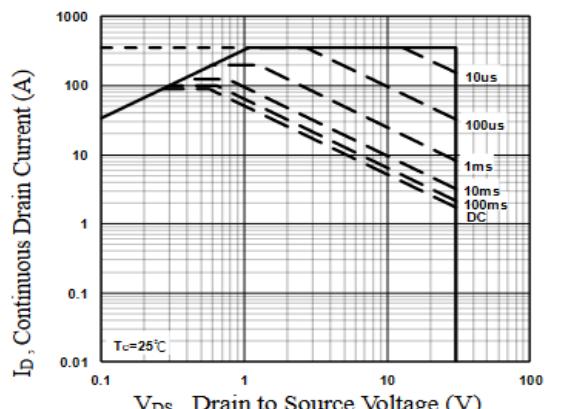


Fig.6 Maximum Safe Operation Area

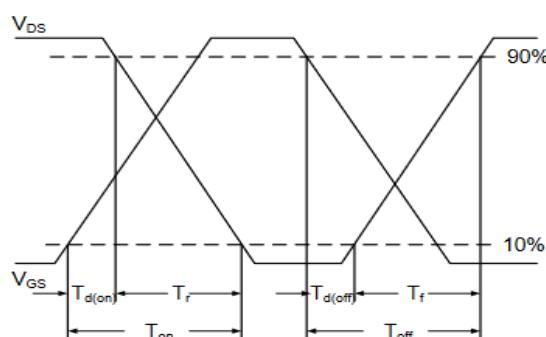
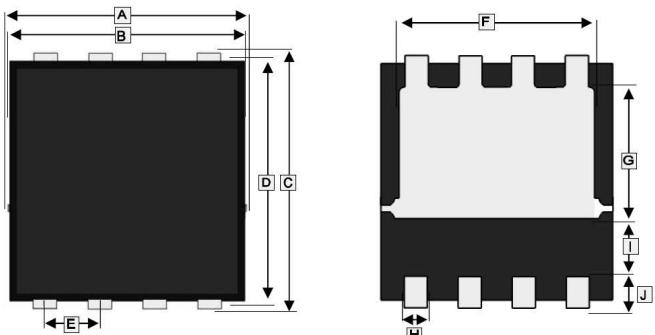


Fig.7 Switching Time Waveform

PACKAGE OUTLINE DIMENSIONS

SPR-8PP

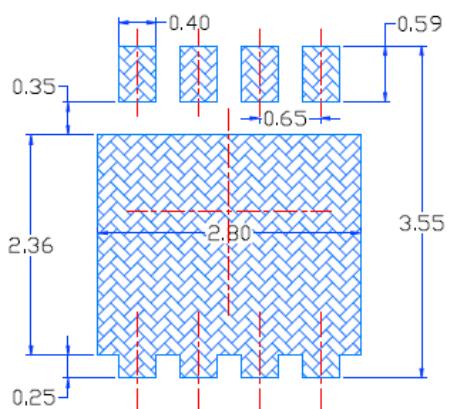


REF.	Millimeter	
	Min.	Max.
A	3.00	3.45
B	3.00	3.25
C	3.00	3.60
D	2.90	3.20
E	0.65 BSC.	
F	2.25	2.69
G	1.35	1.98
H	0.20	0.40
I	0.57	0.87
J	0.30	0.60
K	0.10	0.25
L	0.60	0.90



MOUNTING PAD LAYOUT

SPR-8PP



*Dimensions in millimeters