

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching application.

FEATURES

- Improved dv/dt capability
- Fast switching
- Green Device Available

APPLICATION

- Networking
- Load Switch
- LED applications

MARKING

NG6P0

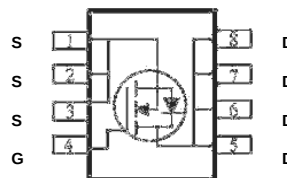
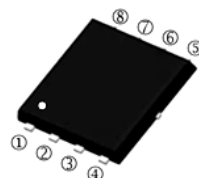
PACKAGE INFORMATION

Package	MPQ	Leader Size
SPR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SSPR66N06-C	Lead (Pb)-free and Halogen-free

SPR-8PP



ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_C=25^\circ\text{C}$	I_D	66	A
Pulsed Drain Current ¹	I_{DM}	90	A
Power Dissipation $T_C=25^\circ\text{C}$	P_D	31.25	W
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	4	

ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	60	-	-	V	V _{GS} =0V, I _D =250μA
Gate-Threshold Voltage	V _{GS(th)}	1.0	-	3	V	V _{DS} =V _{GS} , I _D =250μA
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
Drain-Source Leakage Current	I _{DSS}	-	-	1	μA	V _{DS} =48V, V _{GS} =0V
Static Drain-Source On-Resistance	R _{DS(ON)}	-	-	6	mΩ	V _{GS} =10V, I _D =15A
		-	-	10		V _{GS} =4.5V, I _D =8A
Gate Resistance	R _g	-	2.1	-	Ω	V _{GS} =0V, V _{DS} =0V, f=1MHz
Forward Transconductance	g _{fs}	-	31	-	S	V _{DS} =5V, I _D =20A
Total Gate Charge	Q _g	-	37.4	-	nC	V _{DS} =30V V _{GS} =10V I _D =20A
Gate-Source Charge	Q _{gs}	-	6.5	-		
Gate-Drain Change	Q _{gd}	-	10	-		
Turn-on Delay Time	T _{d(on)}	-	9.5	-	nS	V _{DS} =30V V _{GS} =10V I _D =1A R _G =3Ω
Rise Time	T _r	-	26	-		
Turn-off Delay Time	T _{d(off)}	-	29	-		
Fall Time	T _f	-	19.5	-		
Input Capacitance	C _{iss}	-	2083	-	pF	V _{DS} =30V V _{GS} =0V f=1MHz
Output Capacitance	C _{oss}	-	793	-		
Reverse Transfer Capacitance	C _{rss}	-	16.5	-		
Source-Drain Diode						
Reverse Recovery Time	t _{rr}	-	40	-	A	I _F =20A , V _R =30V , di/dt=100A/us
Reverse Recovery Charge	Q _{rr}	-	48.7	-		
Diode Forward Voltage	V _{SD}	-	-	1.1	V	I _S =1A, V _{GS} =0V

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS

FIG. 1- I_D vs T_C

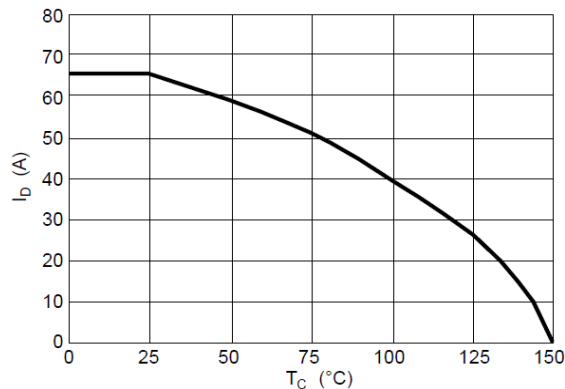


FIG. 2-Normalized $V_{GS(th)}$ vs T_J

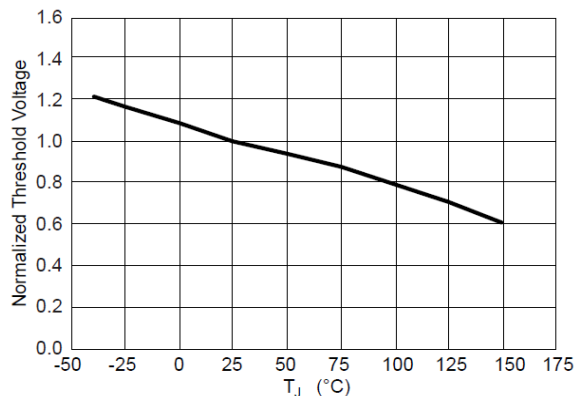


FIG. 3-Normalized $R_{DS(ON)}$ vs T_J

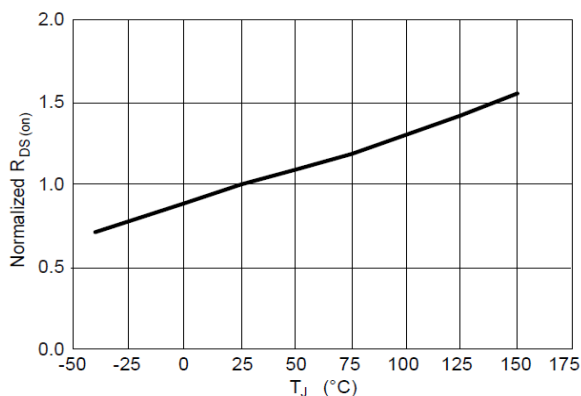


FIG. 4-Gate Charge Characteristics

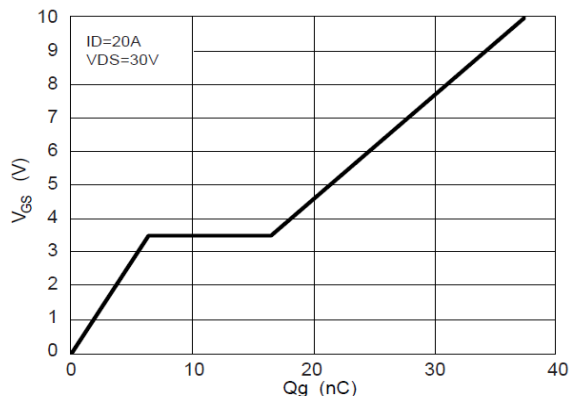


FIG. 5- $R_{DS(ON)}$ vs I_D

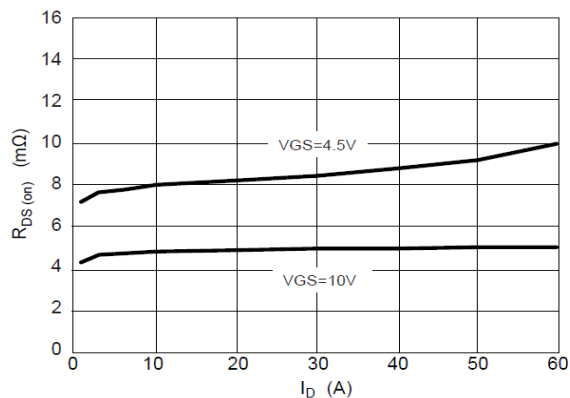


FIG. 6-Power Dissipation

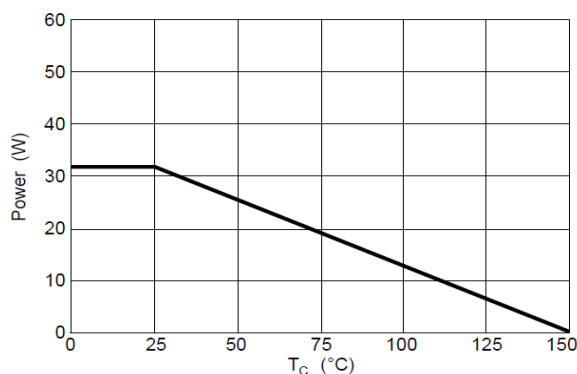


FIG. 7-Switching Time Waveform

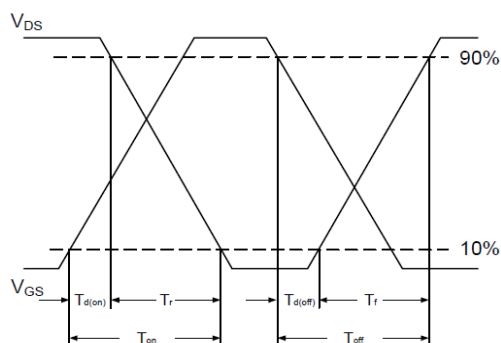
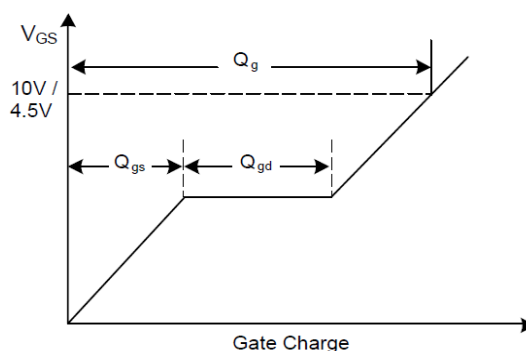
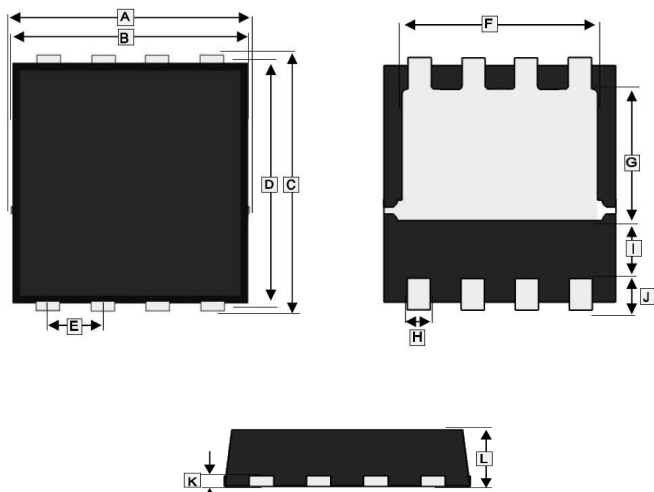


FIG. 8-Gate Charge Waveform



PACKAGE OUTLINE DIMENSIONS

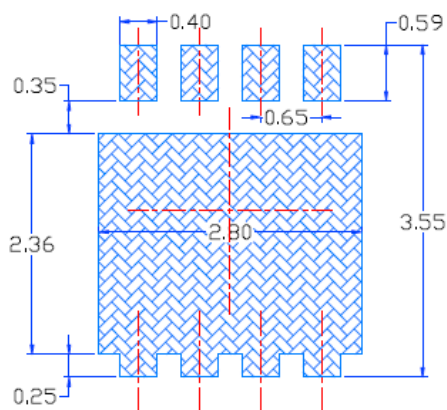
SPR-8PP



REF.	Millimeter	
	Min.	Max.
A	3.00	3.45
B	3.00	3.25
C	3.05	3.50
D	2.90	3.20
E	0.65 BSC.	
F	2.29	2.65
G	1.35	1.98
H	0.20	0.40
I	0.57	0.87
J	0.30	0.60
K	0.10	0.25
L	0.60	0.90

MOUNTING PAD LAYOUT

SPR-8PP



*Dimensions in millimeters