Elektronische Bauelemente

SSG3903-C

-13A, -30V, $R_{DS(ON)}$ 9.5mΩ
P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

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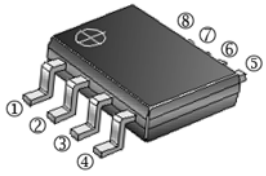


FEATURES

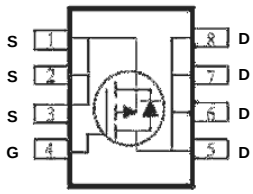
- Fast switching
- Green Device Available

APPLICATIONS

- MB / VGA / Vcore
- LED Application
- Load Switch
- POL Applications

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	3K	13 inch



ORDER INFORMATION

Part Number	Type
SSG3903-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	-13	A
	T_C=100°C		-7.8	
Pulsed Drain Current [1]		I_{DM}	-52	A
Power Dissipation		P_D	4.2	W
Thermal Resistance Junction-Ambient		$R_{\theta JA}$	60	℃/W
Thermal Resistance Junction-Case		$R_{\theta JC}$	30	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-30	-	-	V	V_{GS}=0V, I_D= -250μA
Gate Threshold Voltage		$V_{GS(th)}$	-1	-1.6	-2.5	V	V_{DS}=V_{GS}, I_D= -250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{DS}=0V, V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	-1	μA	V_{DS}= -30V, V_{GS}=0V
	T_J=125°C		-	-	-10		V_{DS}= -24V, V_{GS}=0V
Drain-Source On-Resistance		$R_{DS(ON)}$	-	8	9.5	mΩ	V_{GS}= -10V, I_D= -10A
			-	12.4	15		V_{GS}= -4.5V, I_D= -8A
Gate Resistance		R_G	-	8.5	-	Ω	V_{DS}=V_{GS}=0V, f=1MHz
Forward Transconductance		g_{fs}	-	13	-	S	V_{DS}= -10V, I_D= -10A
Total Gate Charge [2,3]		Q_g	-	35	-	nC	V_{DS}= -15V V_{GS}= -4.5V I_D= -10A
Gate-Source Charge [2,3]		Q_{gs}	-	10.8	-		
Gate-Drain Charge [2,3]		Q_{gd}	-	10.6	-		
Turn-On Delay Time [2,3]		$T_{d(on)}$	-	24.5	-	nS	V_{DD}= -15V V_{GS}= -10V I_D= -1A R_G=6Ω
Rise Time [2,3]		T_r	-	10.5	-		
Turn-Off Delay Time [2,3]		$T_{d(off)}$	-	156.8	-		
Fall Time [2,3]		T_f	-	50	-		
Input Capacitance		C_{iss}	-	3300	-	pF	V_{DS}= -15V V_{GS}=0V f=1MHz
Output Capacitance		C_{oss}	-	410	-		
Reverse Transfer Capacitance		C_{rss}	-	280	-		
Source-Drain Diode							
Diode Forward Voltage		V_{SD}	-	-	-1	V	V_{GS}=0V, I_S= -1A
Continuous Source Current		I_S	-	-	-13	A	V_G=V_D=0V, Force Current
Pulsed Source Current		I_{SM}	-	-	-26		

Notes:

1. Repetitive Rating：Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width≦300us, duty cycle≦2%.
3. Essentially independent of operating temperature.

CHARACTERISTICS CURVES

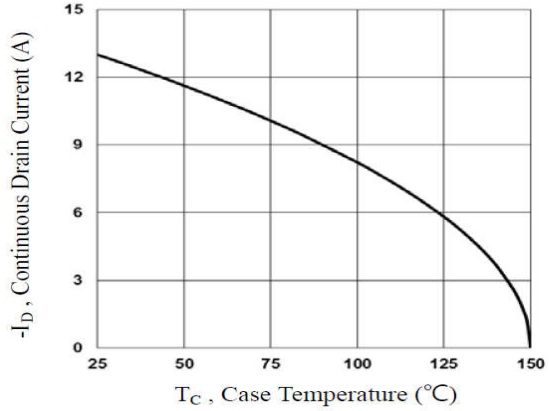


Fig.1 Continuous Drain Current vs. T_C

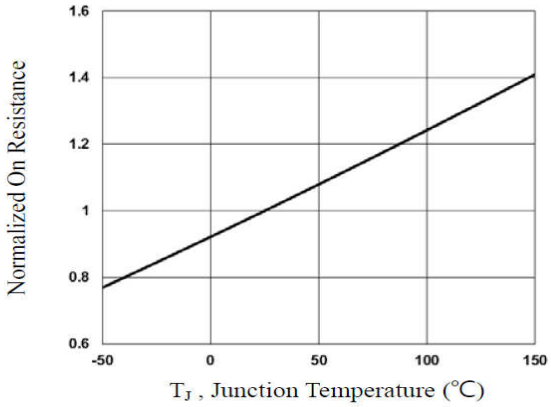


Fig.2 Normalized RDSON vs. T_J

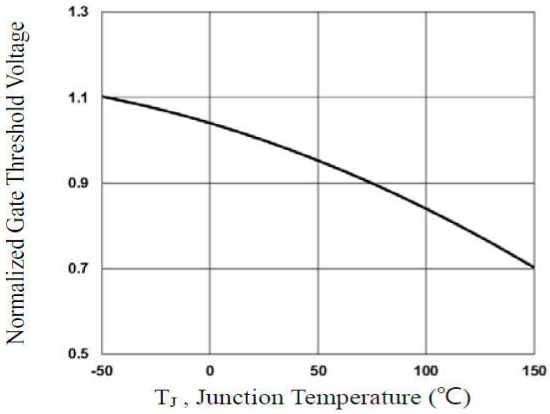


Fig.3 Normalized V_{th} vs. T_J

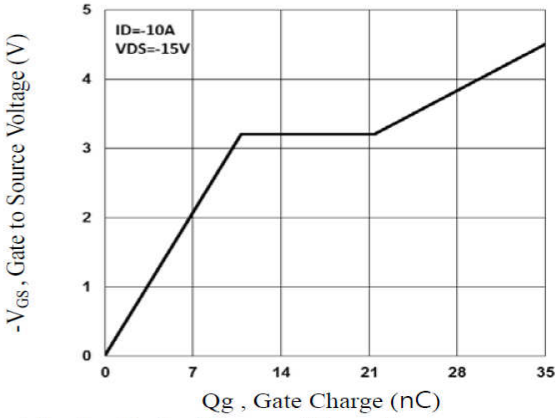


Fig.4 Gate Charge Waveform

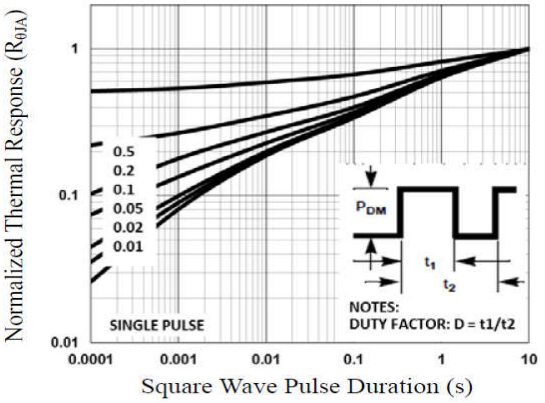


Fig.5 Normalized Transient Impedance

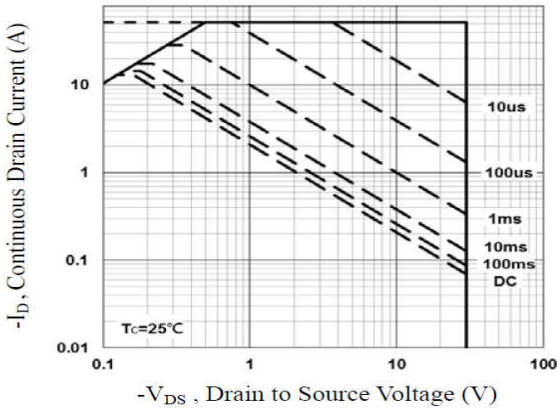


Fig.6 Maximum Safe Operation Area

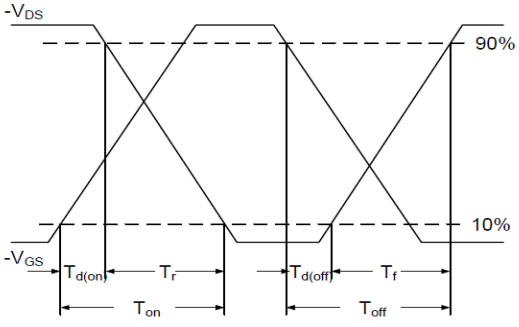


Fig.7 Switching Time Waveform

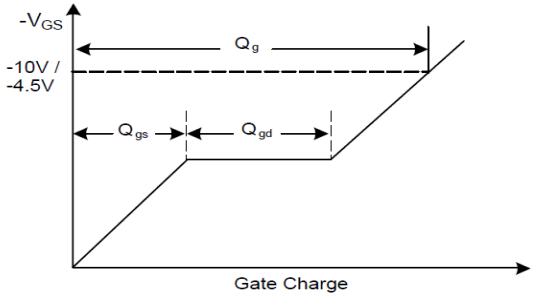


Fig.8 Gate Charge Waveform

PACKAGE OUTLINE DIMENSIONS

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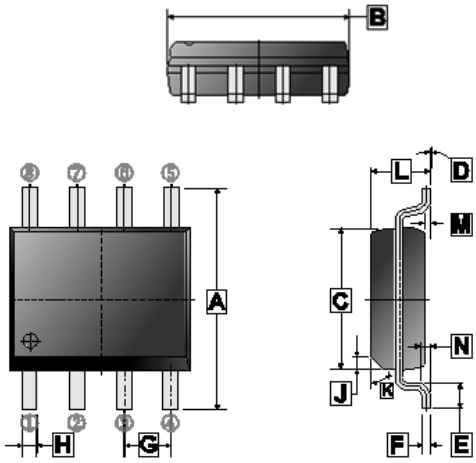

REF.	Millimeter	
	Min.	Max.
A	5.80	6.20
B	4.38	5.20
C	3.70	4.10
D	0°	8°
E	0.40	1.27
F	0.10	0.26
G	1.27 TYP.	
H	0.30	0.51
J	0.375 REF.	
K	45° REF.	
L	1.30	1.80
M	0	0.25
N	0.25 REF.	

MOUNTING PAD LAYOUT

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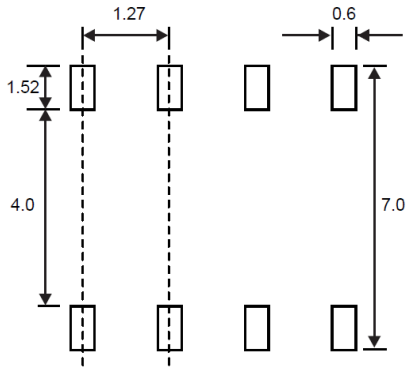

*Dimensions in millimeters