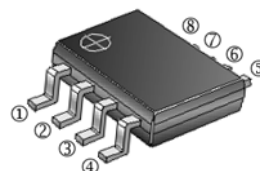


RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

SOP-8



FEATURES

- Fast switching
- Green Device Available

APPLICATIONS

- Motor Driver Applications
- LED Application
- Load Switch
- POL Applications

MARKING

PC4P8

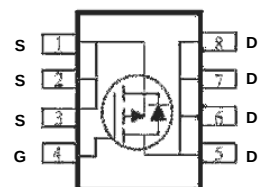
DS3959

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	3K	13 inch

ORDER INFORMATION

Part Number	Type
SSG24P03-C	Lead (Pb)-free and Halogen-free



ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_C=25^\circ\text{C}$	I_D	-24	A
Pulsed Drain Current ¹	I_{DM}	-96	A
Power Dissipation $T_C=25^\circ\text{C}$	P_D	2.1	W
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	60	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	24	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-50~150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ C$ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV _{DSS}	-30	-	-	V	V _{GS} =0V, I _D = -250μA
Gate Threshold Voltage		V _{GS(th)}	-1.2	-1.6	-2.2	V	V _{DS} =V _{GS} , I _D = -250μA
Gate-Source Leakage Current		I _{GSS}	-	-	±100	nA	V _{DS} =0V, V _{GS} = ±20V
Drain-Source Leakage Current	T _J =25°C	I _{DSS}	-	-	-1	μA	V _{DS} = -30V, V _{GS} =0V
	T _J =125°C		-	-	-10		V _{DS} = -24V, V _{GS} =0V
Drain-Source On-Resistance		R _{DS(ON)}	-	3.8	4.8	mΩ	V _{GS} = -10V, I _D = -17.5A
			-	5.8	7.8		V _{GS} = -4.5V, I _D = -10A
Forward Transconductance		g _{fs}	-	25	-	S	V _{DS} = -10V, I _D = -5A
Total Gate Charge ^{2 3}		Q _g	-	108	-	nC	V _{DS} = -15V
Gate-Source Charge ^{2 3}		Q _{gs}	-	15	-		V _{GS} = -10V
Gate-Drain Charge ^{2 3}		Q _{gd}	-	17.4	-		I _D = -10A
Turn-On Delay Time ^{2 3}		T _{d(on)}	-	28	-	nS	V _{DD} = -15V
Rise Time ^{2 3}		T _r	-	16	-		V _{GS} = -10V
Turn-Off Delay Time ^{2 3}		T _{d(off)}	-	178	-		I _D = -1A
Fall Time ^{2 3}		T _f	-	72	-		R _G =6Ω
Input Capacitance		C _{iss}	-	6220	-	pF	V _{DS} = -25V
Output Capacitance		C _{oss}	-	782	-		V _{GS} =0V
Reverse Transfer Capacitance		C _{rss}	-	412	-		f=1MHz
Source-Drain Diode							
Diode Forward Voltage		V _{SD}	-	-	-1	V	V _{GS} =0V, I _S = -1A
Continuous Source Current		I _S	-	-	-24	A	V _G =V _D =0V, Force Current
Pulsed Source Current		I _{SM}	-	-	-48		

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Essentially independent of operating temperature.

CHARACTERISTICS CURVES

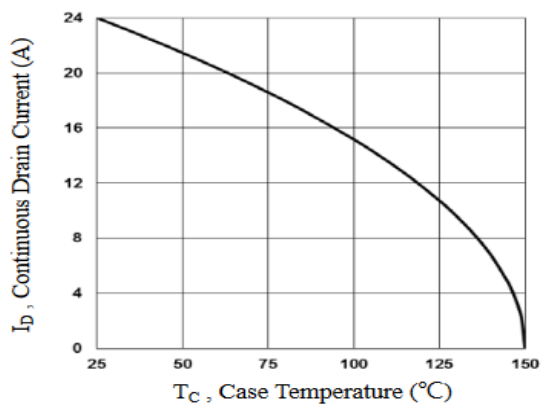


Fig.1 Continuous Drain Current vs. T_C

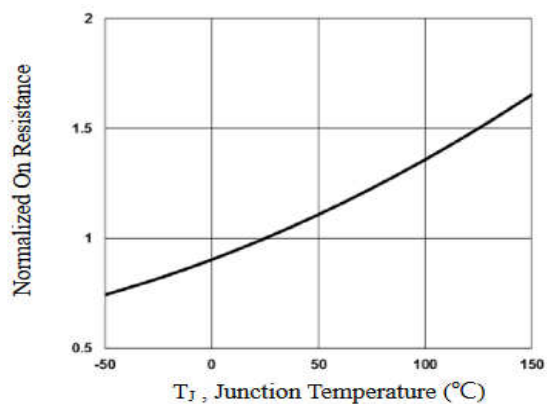


Fig.2 Normalized $R_{DS(ON)}$ vs. T_J

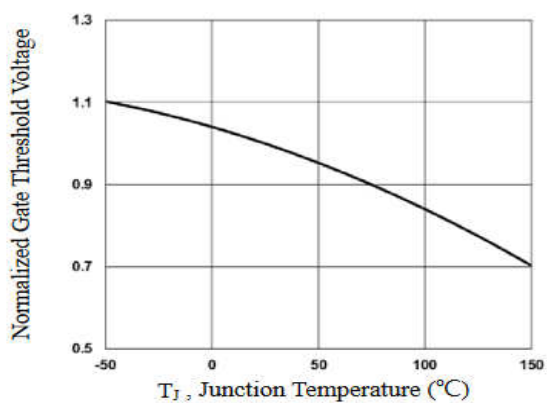


Fig.3 Normalized V_{th} vs. T_J

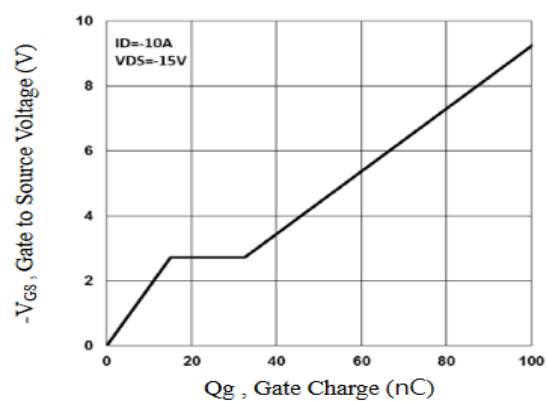


Fig.4 Gate Charge Waveform

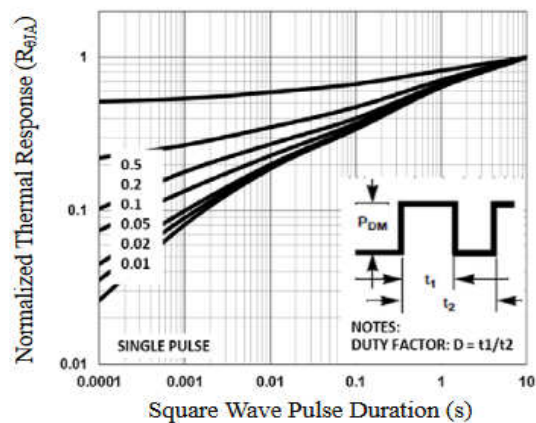


Fig.5 Normalized Transient Impedance

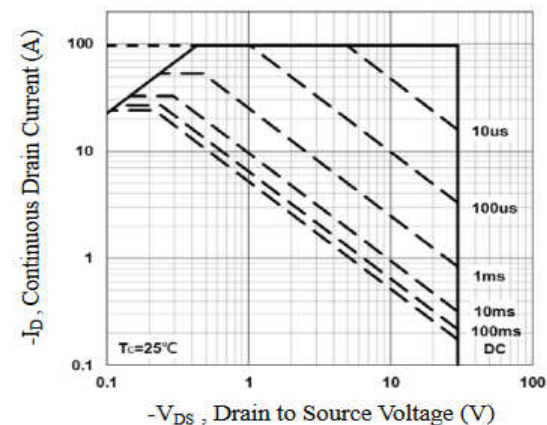


Fig.6 Maximum Safe Operation Area

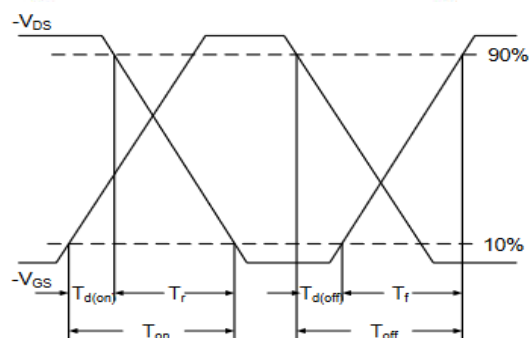


Fig.7 Switching Time Waveform

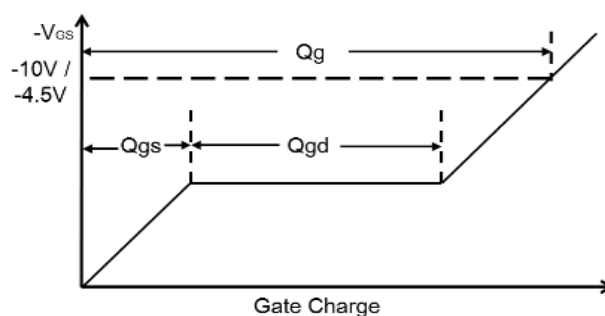
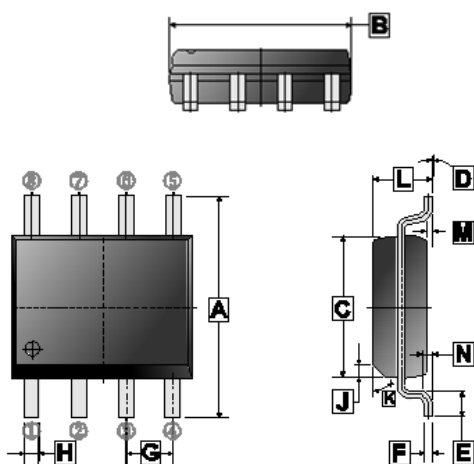


Fig.8 Gate Charge Waveform

PACKAGE OUTLINE DIMENSIONS

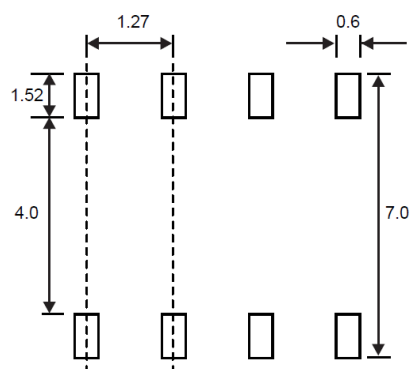
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REF.	Millimeter	
	Min.	Max.
A	5.80	6.20
B	4.38	5.20
C	3.70	4.10
D	0°	8°
E	0.40	1.27
F	0.10	0.26
G	1.27 TYP.	
H	0.30	0.51
J	0.375 REF.	
K	45° REF.	
L	1.30	1.80
M	0	0.25
N	0.25 REF.	

MOUNTING PAD LAYOUT

SOP-8



*Dimensions in millimeters