Elektronische Bauelemente

SSG15N03-C

15A, 30V, $R_{DS(ON)}$ 8.5mΩ
N-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

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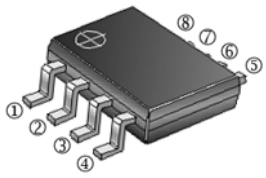


FEATURES

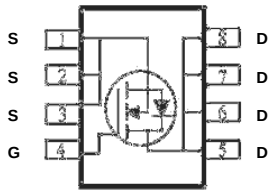
- Fast switching
- Green Device Available

APPLICATIONS

- MB / VGA / Vcore
- POL Applications
- SMPS 2nd SR

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	3K	13 inch



ORDER INFORMATION

Part Number	Type
SSG15N03-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	15	A
	T_C=100℃		9.5	
Pulsed Drain Current [1]		I_{DM}	60	A
Total Power Dissipation	T_C=25℃	P_D	4	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient		$R_{\theta JA}$	85	℃/W
Thermal Resistance Junction-Case		$R_{\theta JC}$	31	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0V, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	1.2	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V, V_{DS}=0V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=24V, V_{GS}=0V
	T_J=125℃		-	-	10		
Static Drain-Source On-Resistance		$R_{DS(ON)}$	-	-	8.5	mΩ	V_{GS}=10V, I_D=15A
			-	-	11		V_{GS}=4.5V, I_D=8A
Gate Resistance		R_g	-	3.2	-	Ω	V_{DS}= V_{GS}=0V, f=1MHz
Forward Transconductance		g_{fs}	-	22	-	S	V_{DS}=10V, I_D=8A
Total Gate Charge		Q_g	-	23.2	-	nC	V_{DS}=15V V_{GS}=10V I_D=1A
Gate-Source Charge		Q_{gs}	-	3.2	-		
Gate-Drain Change		Q_{gd}	-	3.7	-		
Turn-on Delay Time		$T_{d(on)}$	-	7	-	nS	V_{DD}=10V V_{GS}=10V I_D=30A R_G=2.7Ω
Rise Time		T_r	-	76.6	-		
Turn-off Delay Time		$T_{d(off)}$	-	27.1	-		
Fall Time		T_f	-	52.6	-		
Input Capacitance		C_{iss}	-	1180	-	pF	V_{DS}=15V V_{GS}=0V f=1MHz
Output Capacitance		C_{oss}	-	177	-		
Reverse Transfer Capacitance		C_{rss}	-	132	-		
Source-Drain Diode							
Continuous Source Current		I_S	-	-	15	A	V_{GS}=V_{DS}=0V, Force Current
Pulsed Source Current [3]		I_{SM}	-	-	30		
Forward on Voltage [3]		V_{SD}	-	-	1	V	I_S=1A, V_{GS}=0V

Notes:
1. Repetitive rating：pulsed width limited by maximum junction temperature
2. The data tested by pulsed , pulse width≦300μs , duty cycle≦2%.
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS CURVE

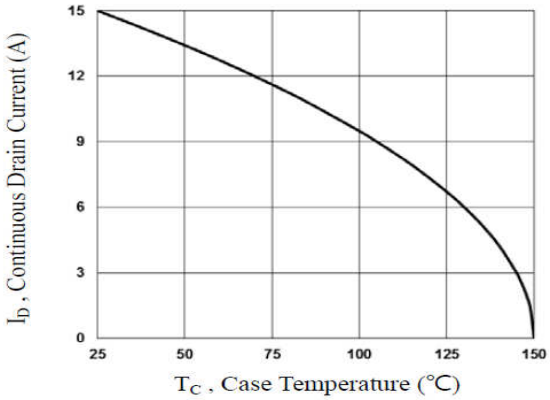


Fig.1 Continuous Drain Current vs. T_C

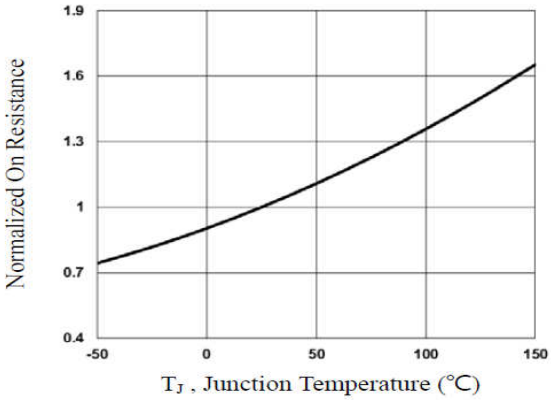


Fig.2 Normalized RDSON vs. T_J

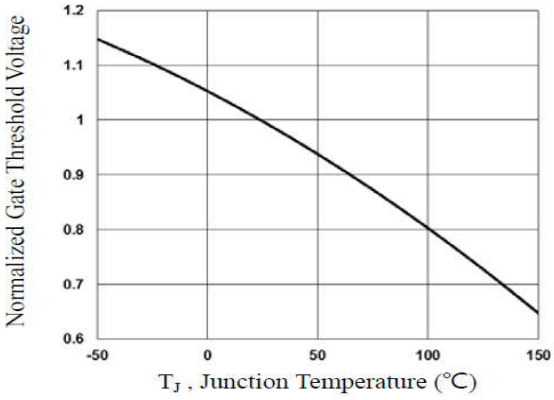


Fig.3 Normalized V_{th} vs. T_J

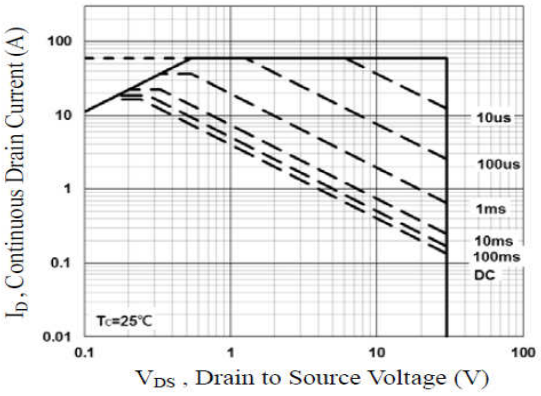


Fig.4 Maximum Safe Operation Area

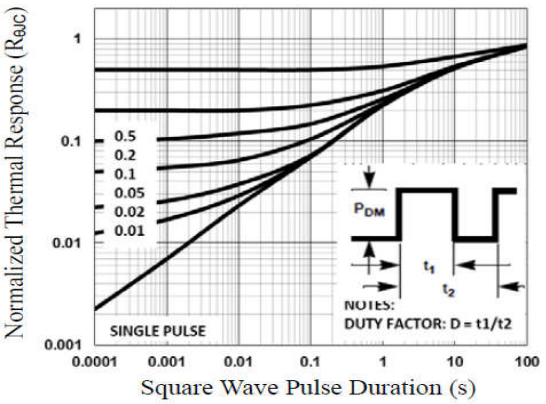


Fig.5 Normalized Transient Impedance

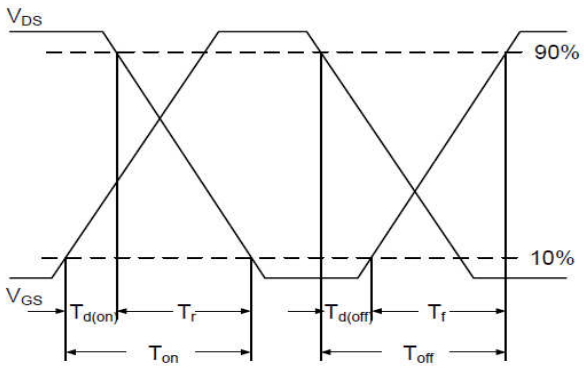


Fig.6 Switching Time Waveform

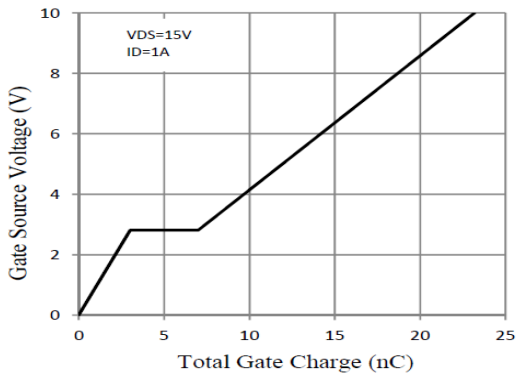


FIG. 7 Gate Charge Characteristics

PACKAGE OUTLINE DIMENSIONS

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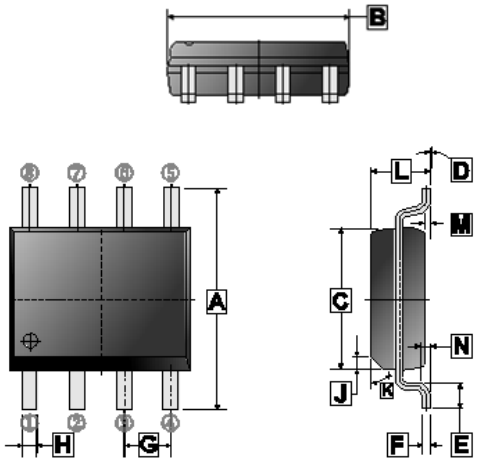

REF.	Millimeter	
	Min.	Max.
A	5.80	6.20
B	4.38	5.20
C	3.70	4.10
D	0°	8°
E	0.40	1.27
F	0.10	0.26
G	1.27 TYP.	
H	0.30	0.51
J	0.375 REF.	
K	45° REF.	
L	1.30	1.80
M	0	0.25
N	0.25 REF.	

MOUNTING PAD LAYOUT

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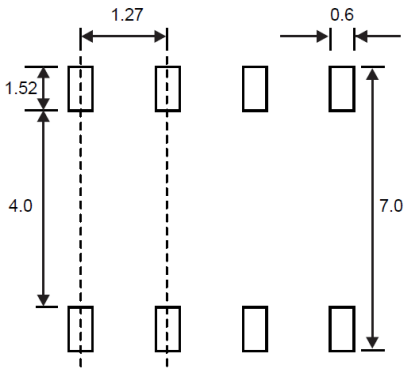

*Dimensions in millimeters