Elektronische Bauelemente

SPR120N10S-C

120A, 100V, $R_{DS(ON)}$ 4.5mΩ

N-Channel Shielded Gate Trench Power MOSFET

RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using SGT MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

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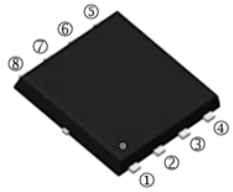


FEATURES

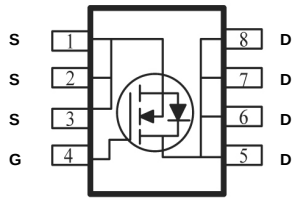
- Improved dv/dt Capability
- Fast Switching
- Green Device Available

APPLICATIONS

- Power Management Switches
- DC/DC Converters

PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch



ORDER INFORMATION

Part Number	Type
SPR120N10S-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	120	A
	T_C=100℃		76	
Pulsed Drain Current [1]		I_{DM}	480	A
Power Dissipation		P_D	131.6	W
Operating Junction & Storage Temperature		T_J, T_{STG}	-55~150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient		$R_{\theta JA}$	48	℃/W
Thermal Resistance Junction-Case		$R_{\theta JC}$	0.95	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage	$V_{GS(th)}$	1.2	1.8	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transfer conductance	g_{fs}	-	70	-	S	V_{DS}=10V, I_D=20A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	V_{DS}=100V, V_{GS}=0
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	-	4.5	mΩ	V_{GS}=10V, I_D=20A
		-	-	6.7	mΩ	V_{GS}=4.5V, I_D=15A
Gate Resistance	R_g	-	1.3	-	Ω	V_{GS}=0, V_{DS}=0V, f=1MHz
Total Gate Charge	Q_g	-	111.2	-	nC	V_{DS}=50V V_{GS}=10V I_D=20A
Gate-Source Charge	Q_{gs}	-	17.5	-		
Gate-Drain Change	Q_{gd}	-	30.2	-		
Turn-on Delay Time	$T_{d(on)}$	-	22.2	-	nS	V_{DS}=50V V_{GS}=10V I_D=20A R_G=3Ω
Rise Time	T_r	-	37.8	-		
Turn-off Delay Time	$T_{d(off)}$	-	95.2	-		
Fall Time	T_f	-	35.6	-		
Input Capacitance	C_{iss}	-	5475	-	pF	V_{DS}=50V V_{GS}=0 f=1MHz
Output Capacitance	C_{oss}	-	768	-		
Reverse Transfer Capacitance	C_{rss}	-	22	-		
Source-Drain Diode						
Diode Forward Voltage	V_{SD}	-	-	1.2	V	I_S=20A, V_{GS}=0
Continuous Source Current	I_S	-	-	120	A	V_G=V_D=0, Force Current
Reverse Recovery Time	T_{rr}	-	59.4	-	nS	I_F=20A,dI/dt=100A/μs
Reverse Recovery Charge	Q_{rr}	-	91.8	-	nC	

Notes:

1. The data tested by pulsed , pulse width≦300μs , duty cycle≦2%
2. Repetitive rating, pulse width limited by junction temperature T_J(MAX) =150℃
3. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

FIG. 1-Output Characteristics

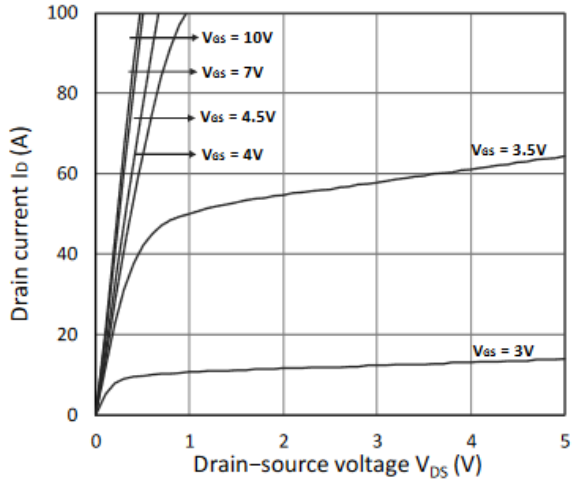


FIG. 2- $R_{DS(ON)}$ vs. I_D

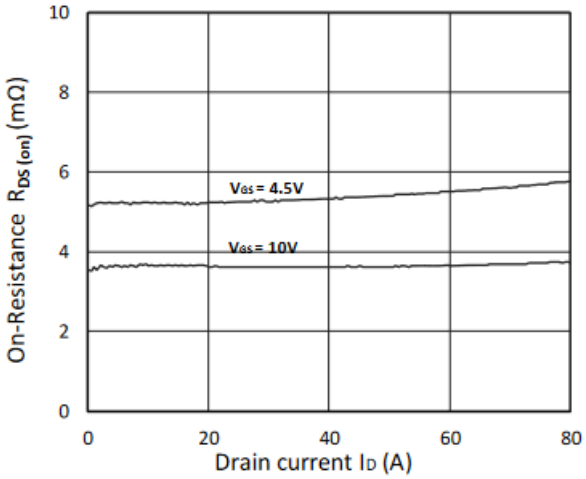


FIG. 3-Gate Charge Characteristics

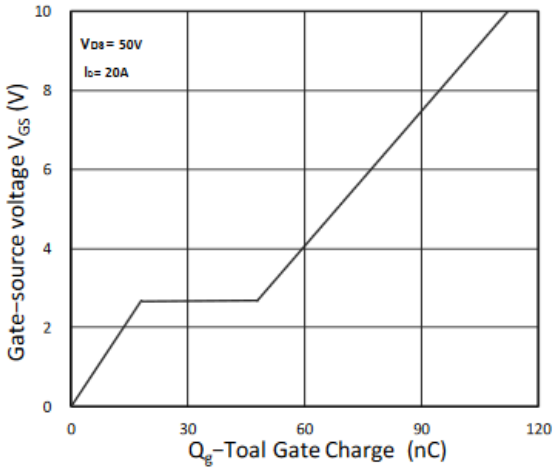


FIG. 4-Safe Operating Area

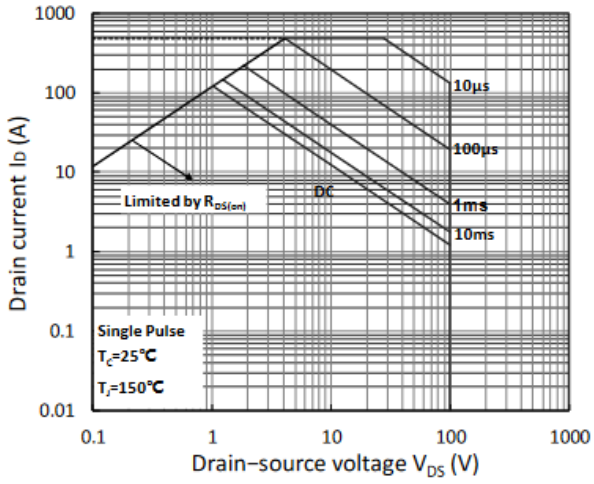
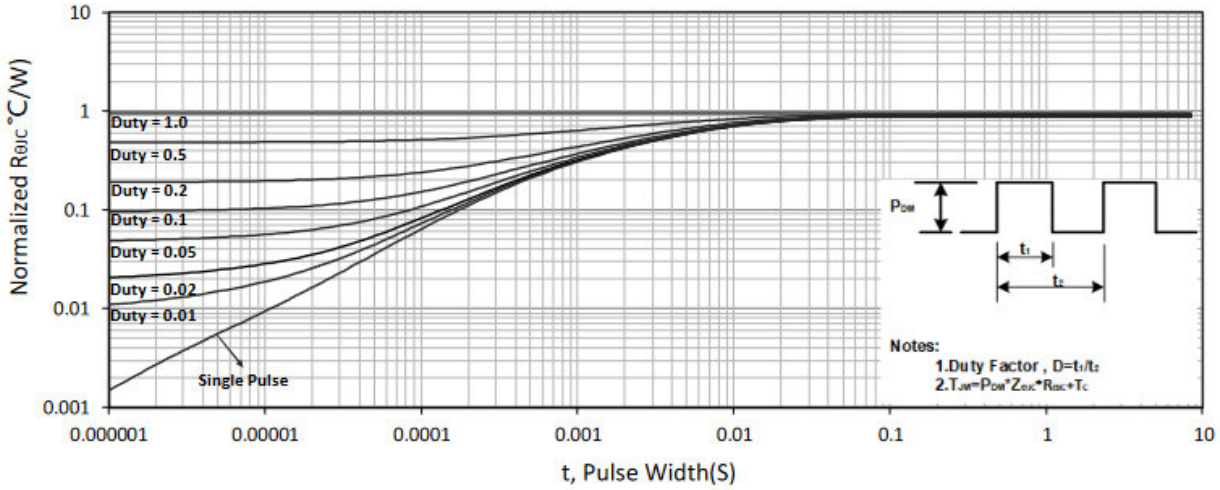


FIG. 5-Normalized Maximum Transient Thermal ImpedanceFigure



PACKAGE OUTLINE DIMENSIONS

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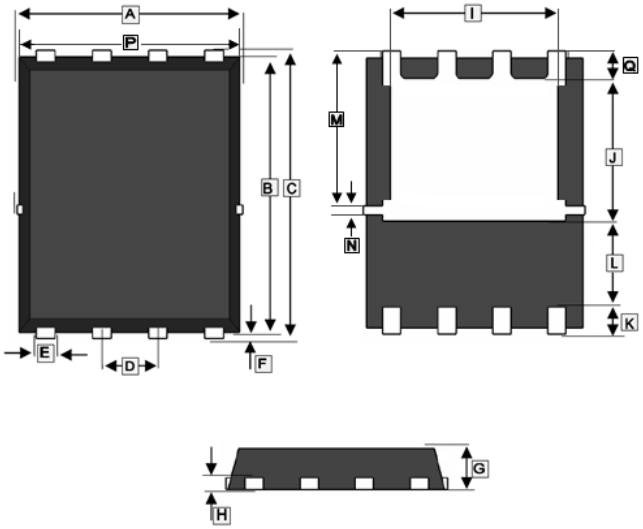
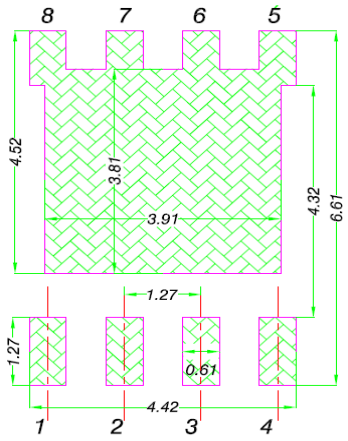


REF.	Millimeter	
	Min.	Max.
A	4.80	5.40
B	5.45	6.06
C	5.80	6.35
D	1.27 BSC.	
E	0.30	0.51
F	0.05	0.36
G	0.80	1.30
H	0.254 REF.	
I	3.80 REF.	
J	3.60 REF.	
K	0.60 REF.	
L	1.10 REF.	
M	3.75 REF.	
N	0.25 REF.	
P	4.80	5.00
Q	0.50 REF.	

MOUNTING PAD LAYOUT

PR-8PP



*Dimensions in millimeters